HAILO

Empowering Intelligence

Hailo-10H Datasheet

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April 2026

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Documentation Control

History Table

Revision	Date	Description
0.5	January 2024	First release
0.6	February 2024	Updated block diagram Added details for industrial version
0.7	April 2024	Updated Section 1.1. Pin Multiplex Specifications
0.8	May 2024	Updated Section 1.1. General Description and Overview. Typo corrections
0.9	January 2025	Updated Section 1.1. Pin Multiplex Specifications Updated Section 3.3. Power up sequence Added Section 1.2. Thermal Design Power USB feature description updated Section 4.4.3. Updated power pin data, Fuse VQPS Factory use only-connect to GND Added PCIe Base Specifications, Rev 3.1a to Section 3.8. Added further data on Thermal Throttling Section 3.4.3.1.
1.0	July 2025	Updated power rail voltage values Section 3.1.1. Power up sequence-updated sequence diagram and T5 VDD changed to VDDIO. Updated T7 description on Table 15
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1.4	April 2026	Updated Power up sequence and diagram 3.3.

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Table of Contents

1. Overview 10
1.1. Introduction 10
1.2. General Description 10
1.3. Features 11
1.4. Block Diagram 12
1.5. Ordering Information 13
1.6. Mechanical Details 13
2. Pinout Description 15
2.1. Pin Assignment 15
2.2. Functional Assignment 17
2.3. Pin Multiplex Specifications 37
2.3.1. GPIO Group [0-1] 38
2.3.2. GPIO Group [2-3] 38
2.3.3. GPIO Group [4-5] 39
2.3.4. GPIO Group [6-7] 39
2.3.5. GPIO Group [8-15] 40
2.3.6. GPIO Group [16-31] 41
2.4. Initial Debug Bus 43
3. Electrical Characteristics 44
3.1. Absolute Maximum Ratings 44
3.1.1. Power Rails 44
3.1.2. Thermal Ratings 45
3.1.3. Thermal Design Power 45
3.2. Recommended Operating Conditions 45
3.3. Power-up Sequence 48
3.4. Power Consumption 50
3.4.1. Maximum Supply Current 50
3.4.2. Power Consumption in Selected Test Cases 50
3.4.3. Power Modes 51
3.4.3.1. Thermal Throttling 51
3.5. Digital I/O DC Characteristics 52
3.6. DDR Characteristics 55
3.6.1. Electrical Operating Conditions 55

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3.6.2. TT Clock-DQS Delay at Nominal Voltage and Temperature 55
3.7. USB 3.1 Characteristics 56
3.8. PCIe Characteristics 56
3.9. RGMII Timing Characteristics 59
3.10. RMII Timing Characteristics 60
3.11. QSPI Timing Characteristics 61
3.12. Reset Timing Characteristics 61
4. System Modes and Usage 62
4.1. Bootstraps 62
4.2. Boot Modes 63
4.2.1. Boot from PCIe 63
4.2.2. Boot from Flash 63
4.2.3. Boot from UART 64
4.3. NN Core 65
4.4. High Bandwidth Interfaces 65
4.4.1. Ethernet 65
4.4.2. PCI Express (PCIe) 66
4.4.3. Universal Serial Bus Interface 67
4.4.4. Network on Chip (NoC) 67
4.5. Low Bandwidth Interfaces 68
4.5.1. Inter-Integrated Circuit (I2C) 68
4.5.2. Quad Serial Peripheral Interface (QSPI) 68
4.5.3. Universal Asynchronous Receiver Transmitter (UART) 68
4.6. MCU 69
4.6.1. Cortex M4 Cores 69
4.6.2. Flash System 69
4.7. Application Processor 69
4.7.1. Cortex A53 70
4.7.2. L2 Memory System 70
4.7.3. Generic Interrupt Controller 70
4.7.4. Generic System Timer 71
4.7.5. Application Processor Watchdog 71
4.8. DDR Controller 71
4.8.1. DDR Direct Memory Access 71

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4.9. System Peripherals 71
4.9.1. Temperature Sensor 71
4.9.2. Voltage Monitor 72
4.9.3. DMA 72
4.9.4. General-Purpose Input Output (GPIO) 72
4.9.5. Watchdog 72
4.9.6. Mailbox 73
4.9.7. Semaphore 73
4.9.8. CRC Hardware Offload Engine 73
4.10. Security System 73
4.10.1. Features 73
4.10.2. Lifecycle Management 73
4.10.3. True Random Number Generator (TRNG) 74
4.10.4. Cryptographic Accelerator 74
4.10.5. Trusted Execution Environment (TEE) 74

List of Figures

Figure 1. Hailo-10H system block diagram 12
Figure 2. Hailo-10H package views 13
Figure 3. Two charts displaying the Hailo-10H ball chart pin assignments 16
Figure 4. Power-up sequence 49
Figure 5. Increasing frequency of thermal throttling decreases chip temperature 52
Figure 6. CLK-DQS Delay for TT @Nominal VT 55
Figure 7. RGMII multiplexing & timing diagram – TX signals 59
Figure 8. RGMII multiplexing & timing diagram – RX signals 60
Figure 9. RMII Timing (Ref_CLK In Mode) 60
Figure 10. Reset Characteristics 61
Figure 11. Boot from Flash 63
Figure 12. Boot from UART 64

List of Tables

Table 1. Glossary of terms 8
Table 2. Part ordering information 13
Table 3. Hailo-10H package dimensions 14
Table 4. Hailo-10H functional pin assignment 17

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Table 5. GPIO Group [0-1] multiplex options 38
Table 6. GPIO Group [2-3] multiplex options 38
Table 7. GPIO Group [4-5] multiplex options 39
Table 8. GPIO Group [6-7] multiplex options 39
Table 9. GPIO Group [8-15] multiplex options 40
Table 10. GPIO Group [16-31] multiplex options 41
Table 11. GPIO [0:5} signal behavior during boot 43
Table 12. Absolute maximum power rail ratings 44
Table 13. Absolute maximum thermal ratings 45
Table 14. Hailo-10H operating ranges 45
Table 15. Power-up Sequence Timing Requirements 49
Table 16. Maximum supply current 50
Table 17. Hysteresis between heating and cooling for each of the threshold crossings 52
Table 18. Failsafe digital pin DC characteristics 53
Table 19. Regular GPIOs DC characteristics 54
Table 20. Electrical operating conditions for LPDDR4 55
Table 21. Electrical operating conditions for LPDDR4X 55
Table 22. PCIe Gen1 transmitter characteristics 56
Table 23. PCIe Gen2 transmitter characteristics 56
Table 24. PCIe Gen3 transmitter characteristics 56
Table 25. PCIe transmitter data rate independent characteristics 57
Table 26. PCIe receiver electrical idle detect threshold 57
Table 27. PCIe receiver termination characteristics 58
Table 28. RGMII Timing Requirements 59
Table 29 . RMII Timing Characteristics 60
Table 30. QSPI Timing Characteristics 61
Table 31. Bootstrap pin names and functions 62

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Glossary

Table 1 provides a useful list of acronyms and abbreviations.

Table 1. Glossary of terms

Abbreviation	Definition
AON	Always on
CMOS	Complementary Metal-Oxide Semiconductor
CS	Chip Select
DDR	Double Data Rate
DMA	Direct Memory Access
DNN	Deep Neural Network
ECC	Error Correction Code
FPS	Frames per Second
FPU	Floating Point Accelerator Unit
GND	Ground
GPIO	General-Purpose Input Output
HS	High Speed
I/O	Input Output
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LVCMOS	Low Voltage CMOS (Technology)
MCU	Microcontroller Unit
MMU	Memory Management Unit
MIPI	Mobile Industry Processor Interface
MPP	Multi Protocol PHY
MPU	Memory Protection Unit
NN	Neural Network
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer
PLL	Phase-Locked Loop

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Abbreviation	Definition
PVT	Process, Voltage, and Temperature
PRCM	Power, Reset and Clock Management
QSPI	Quad Serial Peripheral Interface
SCMI	System Control and Management Interface
SPI	Serial Peripheral Interface
TOPS	Tera Operations Per Second
UART	Universal Asynchronous Receiver Transmitter
VCC	Supply Voltage to Circuit
VDD	Operating Voltage of the Chip
VDDIO	Operating Voltage for I/O Digital Interface

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1. Overview

1.1. Introduction

This datasheet provides a technical description of the Hailo-10H AI accelerator based on Hailo second generation NPU architecture.

1.2. General Description

The Hailo-10H is an AI accelerator that targets edge applications, enabling an immersive vision and generative AI experience on the edge with best-in-class high power efficiency consuming as little as 2.5W in typical AI workloads, all at a low cost.

The Hailo-10H AI accelerator combines Hailo's patented and field proven AI inference capabilities. The unprecedented AI capacity of up to 40 INT4 TOPS allows for high-performance processing of both vision and generative AI models, and efficient execution of multiple complex deep learning AI applications at superior efficiency.

This is thanks to Hailo's market proven unique deep Neural Network (NN) Core processing, based on innovative design elements, physically distributed computation and software abstraction. Furthermore, the Hailo-10H is supported by a robust and mature software suite, backed by the world's largest edge AI community.

Unparalleled AI Analytics

- Up to 40 INT4 TOPS (Tera Operations Per Second) on a powerful Neural Network (NN) Core enabling the processing of advanced DL models.
- High FPS deep learning model processing for faster and highly accurate detection of more objects per frame.
- Best AI performance at a standard low-power consumption & cost envelope.

Flexible and Secure System

- Industry-standard frameworks
- Industrial grade SoC with efficient interfaces for data, and memory.
- Secure boot and secure debug with hardware accelerated crypto library, ARM®TrustZone®, TRNG, and Firewall.

Comprehensive Software Suite

The Hailo-10H AI accelerator software package includes a set of drivers, libraries and tools designed to develop advanced AI applications.

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1.3. Features

- High-performance Hailo NN core sub-system
  - Hailo's patented structure defined dataflow architecture
  - 40 INT4 TOPS
  - Full software suite for continuous capabilities upgrades
- AP sub-system
  - Quad-cores ARM® Cortex® A53@1.3 GHz 12 kDMIPS
- MCU sub-system
  - 2x Cortex M4 @ 200MHz
- Memory Interfaces
  - LPDDR4/4X 32-bit @4266 MT/s
  - Flash controller: SPI/DSPI/QSPI up to 4 devices
- Peripheral Interfaces
  - PCIe® Gen 3.0 x4 lanes
  - 10 / 100 / 1000 Mbit/s Ethernet with RMII / RGMII
  - USB3.1 Gen2 Host/Device
  - I2C: 4 interfaces
  - GPIOs: 32 pins
  - UART: 4 interfaces
- System Control & Debug
  - JTAG, Timers, Monitors
- General Purpose DMA 16 channels
- Security
  - Secure boot, Secure debug
  - HW accelerated crypto library
  - ARM®TrustZone®, TRNG, Firewall
- Physical
  - Packaging: FCCSP 15x15 mm^2
  - Operating temperature -40 to 85 °C

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1.4. Block Diagram

The subsystems and functional modules of the Hailo-10H SoC are displayed in the block diagram below.

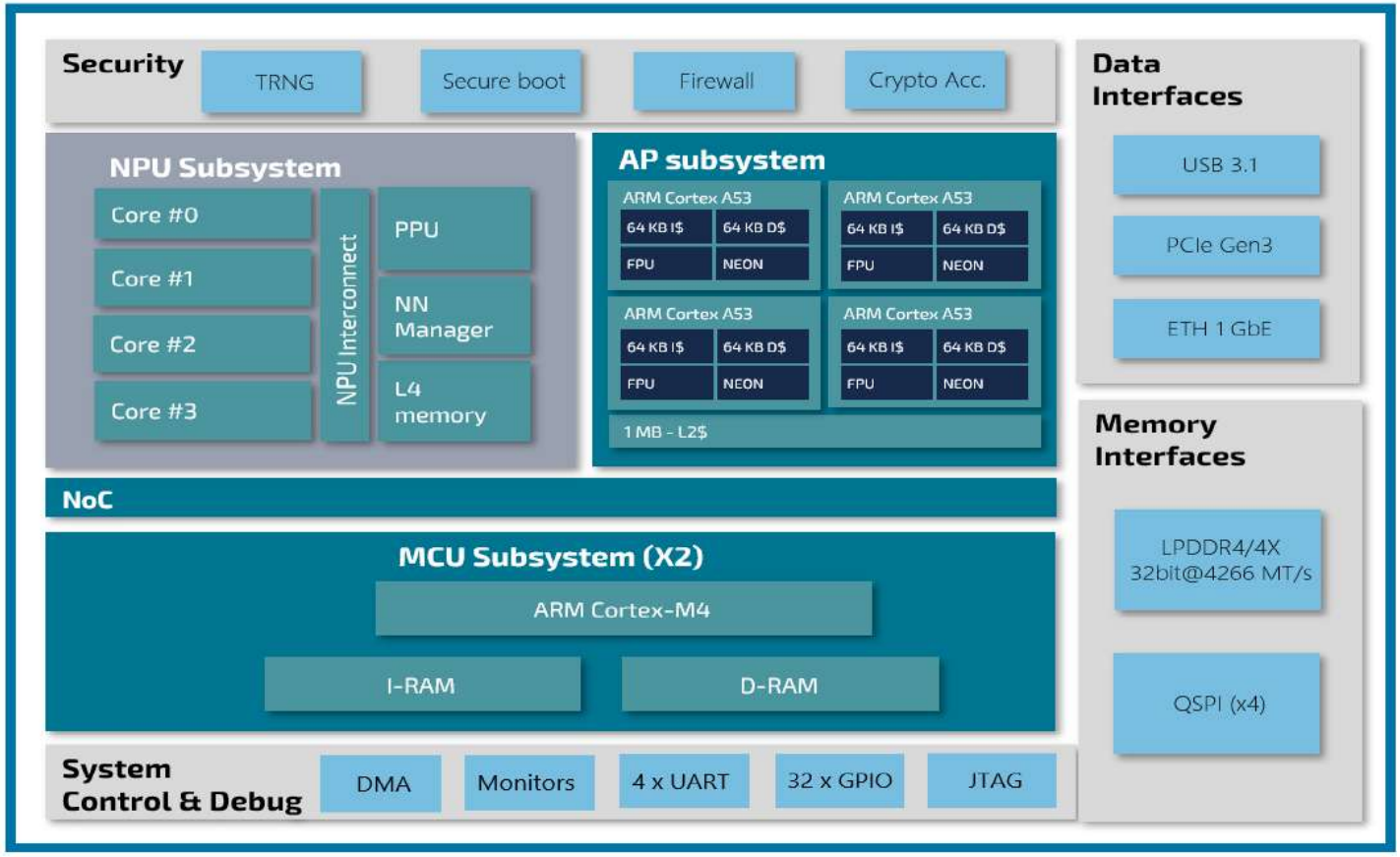


Figure 1. Hailo-10H system block diagram

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1.5. Ordering Information

Table 2. Part ordering information

Part Number	Device Grade	Operating Temperature Range
HNC2HBI11SM	Hailo-10H Industrial Version IC	-40 to 85 °C

1.6. Mechanical Details

The top, side and bottom views of the 484-pin FCCSP package are displayed in Figure 2 and Table 3 lists the package dimensions.

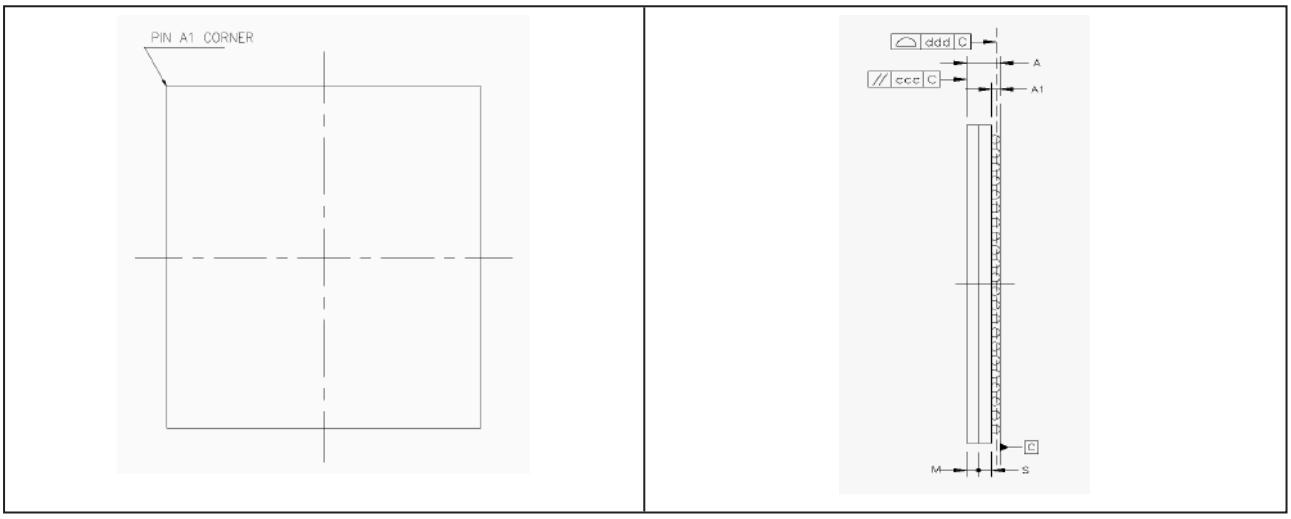


Figure 2. Hailo-10H package views

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Table 3. Hailo-10H package dimensions

Description	Symbol		Common Dimensions		
			Min	Nom	Max
Package			FCCSP		
Total thickness	A		-	-	1.400
Mold Thickness	M		0.450 Ref		
Stand-off	A1		0.270	-	0.370
Substrate Thickness	S		0.388 Ref		
Body size	X	E	15,000 BSC		
	Y	D	15,000 BSC		
Ball diameter			0.400		
Ball width	b		0.350	-	0.450
Ball pitch	e		0.65		
Ball count	n		484		
Edge ball center to center	X	E1	13.650 BSC		
	Y	D1	13.650 BSC		
Package edge tolerance	aaa		0.150		
Hold parallelism	ccc		0.200		
Coplanarity	ddd		0.120		
Ball offset (package)	eee		0.150		
Ball offset (ball)	fff		0.080		

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2. Pinout Description

2.1. Pin Assignment

The following two pages display the pin layout and coordinates for the Hailo-10H ball chart pin assignments.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	DDR_DQ0	DDR_DQ1	GND	GND	MPP_TX3_P	MPP_RX3_P	MPP_TX2_P	MPP_RX2_P	MPP_REFCLK_P	MPP_RX1_P	MPP_TX1_P	MPP_RX0_P
B	DDR_DQS0_P	DDR_DQS0_N	DDR_DQ3	GND	GND	MPP_TX3_N	MPP_RX3_N	MPP_TX2_N	MPP_RX2_N	MPP_REFCLK_N	MPP_RX1_N	MPP_TX1_N	MPP_RX0_N
C	DDR_DQ7	DDR_DM0	DDR_DQ4	DDR_VDDQX	GND	MPP_AVDD_C	MPP_AVDD_C	MPP_AVDD_D	MPP_AVDD_D	PCIE_PERST_N	PCIE_WAKE_N	MPP_AVDD_D	MPP_AVDD_D
D	DDR_DQ2	DDR_DQ6	DDR_DQ5	DDR_VDDQX	GND	GND	GND	GND	MPP_AVDD_D	PCIE_CMN_REXT	PCIE_CLKREQ_N	MPP_AVDD_D	GND
E	DDR_DQ15	DDR_DQ12	DDR_DQ14	DDR_VDDQX	GND	USB_VBUS	NC	NC	GND	GND	GND	GND	GND
F	DDR_DQS1_P	DDR_DQS1_N	DDR_DQ11	GND	GND	USB_AVDD_IO	NC	NC	GND	GND	AVDD_TS	AVDD_VM	GND
G	DDR_DQ8	DDR_DQ9	DDR_DM1	DDR_VDDQ	GND	USB_AVDD_CORE	GND	USB_AVDD_IO_HV	GND	GND	GND	GND	GND
H	DDR_DQ13	DDR_DQ10	DDR_CS0_N	DDR_VDDQ	GND	DDR_VDDQ	GND	DDR_VDD	VDD	GND	VDD	VDD	GND
J	DDR_CA0	DDR_CKE0	DDR_CS1_N	DDR_VDDQ	GND	DDR_VDDQ	GND	DDR_VDD	VDD	GND	VDD	VDD	GND
K	DDR_CA5	DDR_CA2	DDR_CA1	DDR_VDDQ	GND	DDR_VDDQ	GND	DDR_VDD	VDD	GND	VDD	VDD	GND
L	GND	DDR_CA4	DDR_CA3	DDR_VDD	GND	DDR_VDDPLL	GND	DDR_VDD	VDD	GND	VDD	VDD	GND
M	DDR_CLK_N	DDR_CAL0	DDR_ATB0	DDR_ATB1	GND	DDR_VDD	GND	DDR_VDD	VDD	GND	PLL_VDDA	VDD	GND
N	DDR_CLK	DDR_CKE1	DDR_RESET_N	DDR_VDD	GND	DDR_VDD	GND	DDR_VDD	VDD	GND	PLL_VSSA	VDD	GND
P	GND	DDR_DATA_RET	DDR_CS2_N	DDR_VDDQ	GND	DDR_VDD	GND	DDR_VDD	VDD	GND	VDD	VDD	GND
R	DDR_DQ23	DDR_DQ22	DDR_CS3_N	DDR_VDDQ	GND	DDR_VDDQ	GND	DDR_VDD	VDD	GND	VDD	VDD	GND
T	DDR_DM2	DDR_DQ21	DDR_DQ19	DDR_VDDQ	GND	DDR_VDDQ	GND	DDR_PLL_VSSA	DDR_PLL_VDDA	GND	GND	VDD	GND
U	DDR_DQS2_N	DDR_DQS2_P	DDR_DQ20	DDR_VDDQ_CK	GND	DDR_VDDQ	GND	GND	GND	GND	GND	GND	GND
V	DDR_DQ16	DDR_DQ17	DDR_DQ18	DDR_VDDQX	GND	GND	GND	GND	GND	GND	GND	GND	GND
W	DDR_DQ26	DDR_DQ29	DDR_DQ28	DDR_VDDQX	GND	GND	GND	GND	GND	GND	GND	GND	GND
Y	DDR_DQS3_P	DDR_DQS3_N	DDR_DQ27	DDR_VDDQX	GND	GND	GND	GND	GND	GND	GND	GND	GND
AA	DDR_DQ31	DDR_DM3	DDR_DQ25	GND	GND	NC	NC	NC	NC	NC	NC	NC	NC
AB	GND	DDR_DQ30	DDR_DQ24	GND	GND	NC	NC	NC	NC	NC	NC	NC	NC

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	14	15	16	17	18	19	20	21	22
A	MPP_TX0_P	GND	I2C1_SCL	NC	GND	GND	GND	JTAG_TCK	GND
B	MPP_TX0_N	GND	I2C1_SDA	NC	GND	GND	GND	JTAG_TDI	JTAG_TMS
C	GND	MPP_AVDD_C	I2C0_SCL	NC	GND	GND	GND	JTAG_TDO	JTAG_TRSTN
D	MPP_AVDD_H	MPP_AVDD_C	I2C0_SDA	IO_BSO	GND	GND	GND	SPI_DQ2	SPI_DQ0
E	GND	GND	GND	VDDIO	VDDIO	GND	RESET_N	SPI_DQ3	SPI_DQ1
F	GND	GND	GND	GND	GND	UART1_TXD	UART0_TXD	SPI_CS0_N	SPI_SCLK
G	GND	VDD	GND	VDDIO	VDDIO	UART1_RXD	UART0_RXD	SPI_CS1_N	SPI_RESET
H	VDD	VDD	GND	VDDIO	VDDIO	RSVD	SAFETY_ERROR	GND	OSC_XOUT
J	VDD	VDD	GND	GND	GND	RSVD	SAFETY_FATAL	GND	OSC_XIN
K	VDD	VDD	GND	GND	GND	RSVD	ETH_RGMII_TXD2	ETH_RGMII_TXD1	ETH_RGMII_TXD3
L	VDD	VDD	GND	GND	GND	FUSE_VQPS	ETH_RGMII_TX_CTL	ETH_RGMII_TXD0	ETH_RGMII_TX_CLK
M	VDD	VDDIO	GND	GND	GND	ETH_MDIO	ETH_RGMII_RXD2	ETH_RGMII_RXD1	ETH_RGMII_RXD3
N	VDD	VDD	GND	GND	GND	ETH_MDC	ETH_RGMII_RX_CTL	ETH_RGMII_RXD0	ETH_RGMII_RX_CLK
P	VDD	VDD	GND	GND	GPIO_0	GPIO_1	GPIO_2	GPIO_3	GPIO_4
R	VDD	VDD	GND	GND	GPIO_9	GPIO_8	GPIO_7	GPIO_6	GPIO_5
T	GND	VDD	GND	GND	GPIO_10	GPIO_11	GPIO_12	GPIO_13	GPIO_14
U	GND	GND	GND	GND	GPIO_19	GPIO_18	GPIO_17	GPIO_16	GPIO_15
V	GND	GND	GND	GND	GPIO_20	GPIO_21	GPIO_22	GPIO_23	GPIO_24
W	GND	GND	GND	GND	GND	GPIO_28	GPIO_27	GPIO_26	GPIO_25
Y	GND	GND	GND	GND	GND	GND	GPIO_29	GPIO_30	GPIO_31
AA	NC	NC	NC	NC	NC	NC	NC	GND	NC
AB	NC	NC	NC	NC	NC	NC	NC	GND	GND

Figure 3. Two charts displaying the Hailo-10H ball chart pin assignments

Color	Cell Type Power
Green	Ground pin
Pink	Power rail pin
Orange	Functional pin

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2.2. Functional Assignment

Hailo-10H functional pin assignment is described below in Table 4

Pin Types are categorized as follows:

- Power - SoC power rails
- I - input signals (Analog/LVCMOS)
- O - output signals (Analog/LVCMOS)
- OD - Open Drain IO

Table 4. Hailo-10H functional pin assignment

Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
Main Power and Sensing							
A1, A4, A5, A15, A18, A19, A20, A22, B4, B5, B15, B18, B19, B20, C5, C14, C18, C19, C20, D5, D6, D7, D8, D13, D18, D19, D20, E5, E9, E10, E11, E12, E13, E14, E15, E16, E19, F4, F5, F9, F10, F13, F14, F15, F16, F17, F18, G5, G7, G9, G10, G11, G12, G13, G14, G16, H5, H7, H10, H13, H16, H21, J5, J7, J10, J13, J16, J17, J18, J21, K5, K7, K10, K13,	GND		Digital ground for device		Power		

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
K16, K17, K18, L1, L5, L7, L10, L13, L16, L17, L18, M5, M7, M10, M13, M16, M17, M18, N5, N7, N10, N13, N16, N17, N18, P1, P5, P7, P10, P13, P16, P17, R5, R7, R10, R13, R16, R17, T5, T7, T10, T11, T13, T14, T16, T17, U5, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, W5, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, W16, W17, W18, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, AA4, AA5, AA21, AB1, AB4, AB5, AB21, AB22	GND		Digital ground for device		Power		
A17, B17, C17, E7, E8, F7, F8, AA6, AA7, AA8, AA9, AA10, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA22, AB7, AB8, AB9, AB10, AB12, AB13, AB14, AB15, AA11, AB6, AB11,AB16, AB17, AB18, AB19, AB20,	NC		Not connected		NC		

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
G15, H9, H11, H12, H14, H15, J9, J11, J12, J14, J15, K9, K11, K12, K14, K15, L9, L11, L12, L14, L15, M9, M12, M14, N9, N12, N14, N15, P9, P11, P12, P14, P15, R9, R11, R12, R14, R15, T12, T15	VDD		Digital CMOS supply of SoC		Power		
E17, E18, G17, G18, H17, H18, M15	VDDIO		Digital supply for IO pads		Power		
N11	PLL_VSSA		Analog ground for PLL		Power		
M11	PLL_VDDA		Analog supply for PLL		Power		
T9	DDR_PLL_VDDA		Analog supply for the internal DDR PLL		Power		
T8	DDR_PLL_VSSA		Analog ground for the internal DDR PLL		Power		
F11	AVDD_TS		Analog supply for temperature sensor		Power		
F12	AVDD_VM		Analog supply for voltage sensor		Power		
L19	FUSE _VQPS		Power pin for fuse programming		Power		
MPP – Multiple Protocol PHY, for PCI Express (PCIe) and USB3.1 Interfaces							
C11	PCIE_WAKE_N	I	PCIe wake signal to host		LVCMOS		MPP_VDD_H
D11	PCIE_CLKREQ_N	O	PCIe clock request to host	Drive 0	LVCMOS		MPP_VDD_H
C10	PCIE_PERST_N	I	PCIe reset in	PD	LVCMOS	Yes	MPP_VDD_H
D10	PCIE_CMN_REXT	I	PCIe calibration connection to external resistor		Analog		MPP_VDD_H
A14	MPP_TX0_P	O	PCIE TX lane 0 positive signal of data transmit diff-pair		Analog		MPP_VDD_H

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
A12	MPP_TX1_P	O	PCIE TX lane 1 positive signal of data transmit diff-pair		Analog		MPP_VDD_H
A8	MPP_TX2_P	O	PCIE TX lane 2 positive signal of data transmit diff-pair		Analog		MPP_VDD_H
A6	MPP_TX3_P	O	PCIE TX lane 3 positive signal of data transmit diff-pair/ USB 3.1 TX lane 3 positive signal of data transmit diff-pair		Analog		MPP_VDD_H
B14	MPP_TX0_N	O	PCIE TX lane 0 negative signal of data transmit diff-pair		Analog		MPP_VDD_H
B12	MPP_TX1_N	O	PCIE TX lane 1 negative signal of data transmit diff-pair		Analog		MPP_VDD_H
B8	MPP_TX2_N	O	PCIE TX lane 1 negative signal of data transmit diff-pair		Analog		MPP_VDD_H
B6	MPP_TX3_N	O	PCIE TX lane 3 negative signal of data transmit diff-pair/ USB 3.1 TXlane 3 negative signal of data transmit diff-pair		Analog		MPP_VDD_H
A13	MPP_RX0_P	I	PCIE RX lane 0 positive signal of the data receive diff-pair		Analog		MPP_VDD_H
A11	MPP_RX1_P	I	PCIE RX lane 1 positive signal of the data receive diff-pair		Analog		MPP_VDD_H

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
A9	MPP_RX2_P	I	PCIE RX lane 2 positive signal of the data receive diff-pair		Analog		MPP_VDD_H
A7	MPP_RX3_P	I	PCIE RX lane 3 positive signal of the data receive diff-pair/ USB 3.1 RX lane 3 positive signal of the data receive diff-pair		Analog		MPP_VDD_H
B13	MPP_RX0_N	I	PCIE RX lane 0 negative signal of data receive diff-pair		Analog		MPP_VDD_H
B11	MPP_RX1_N	I	PCIE RX lane 1 negative signal of data receive diff-pair		Analog		MPP_VDD_H
B9	MPP_RX2_N	I	PCIE RX lane 2 negative signal of data receive diff-pair		Analog		MPP_VDD_H
B7	MPP_RX3_N	I	PCIE RX lane 3 negative signal of data receive diff-pair/ USB 3.1 RX lane 3 negative signal of data receive diff-pair		Analog		MPP_VDD_H
B10	MPP_REFCLK_N	I	MPP ref clock in negative				
A10	MPP_ REFCLK_P	I	MPP ref clock in positive				
C6, C7, C15, D15	MPP_AVDD_C		Analog power for high-speed clock and LVCMOS functions		Power		
C8, C9, C12, C13, D9, D12,	MPP_AVDD_D		Clean analog power for high-speed clock		Power		
D14	MPP_AVDD_H		PCIe Analog I/O voltage		Power		

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
DDR Interface							
H8, J8, K8, L4, L8, M6, M8, N4, N6, N8, P6, P8 R8	DDR_VDD		DDR core supply voltage		Power		
G4, H4, H6, J4, J6, K4, K6, P4, R4, R6, T4, T6, U6	DDR_VDDQ		DDR I/O driver supply		Power		
C4, D4, E4, V4, W4, Y4	DDR_VDDQX		DDR I/O pre-driver supply for LPDDRX		Power		
L6	DDR_VDDPLL		DDR PLL analog supply		Power		
U4	DDR_VDDQ_CK		IO power for DDR Memory Clock Bit (MCB) macro		Power		
A2	DDR_DQ0	I/O	Bi-directional data bus		Analog		DDR_ VDDQ/DDR_ VDDQX
A3	DDR_DQ1	I/O	Bi-directional data bus		Analog		DDR_ VDDQ/DDR_ VDDQX
D1	DDR_DQ2	I/O	Bi-directional data bus		Analog		DDR_ VDDQ/DDR_ VDDQX
B3	DDR_DQ3	I/O	Bi-directional data bus		Analog		DDR_ VDDQ/DDR_ VDDQX

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
C3	DDR_DQ4	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
D3	DDR_DQ5	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
D2	DDR_DQ6	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
C1	DDR_DQ7	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
G1	DDR_DQ8	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
G2	DDR_DQ9	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
H2	DDR_DQ10	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
F3	DDR_DQ11	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
E2	DDR_DQ12	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
H1	DDR_DQ13	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
E3	DDR_DQ14	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
E1	DDR_DQ15	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
V1	DDR_DQ16	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
V2	DDR_DQ17	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
V3	DDR_DQ18	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
T3	DDR_DQ19	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
U3	DDR_DQ20	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
T2	DDR_DQ21	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
R2	DDR_DQ22	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
R1	DDR_DQ23	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
AB3	DDR_DQ24	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
AA3	DDR_DQ25	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
W1	DDR_DQ26	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX
Y3	DDR_DQ27	I/O	Bi-directional data bus		Analog		DDR_VDDQ/DDR_VDDQX

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
W3	DDR_DQ28	I/O	Bi-directional data bus		Analog		DDR_ VDDQ/DDR_ VDDQX
W2	DDR_DQ29	I/O	Bi-directional data bus		Analog		DDR_ VDDQ/DDR_ VDDQX
AB2	DDR_DQ30	I/O	Bi-directional data bus		Analog		DDR_ VDDQ/DDR_ VDDQX
AA1	DDR_DQ31	I/O	Bi-directional data bus		Analog		DDR_ VDDQ/DDR_ VDDQX
B2	DDR_DQS0_N	I/O	Bi- directional differential output clock signals used to strobe data during READ or Write from\to memory		Analog		DDR_ VDDQ/DDR_ VDDQX
F2	DDR_DQS1_N	I/O	Bi- directional differential output clock signals used to strobe data during READ or Write from\to memory		Analog		DDR_ VDDQ/DDR_ VDDQX
U1	DDR_DQS2_N	I/O	Bi- directional differential output clock signals used to strobe data during READ or Write from\to memory		Analog		DDR_ VDDQ/DDR_ VDDQX
Y2	DDR_DQS3_N	I/O	Bi- directional differential output clock signals used to strobe data during READ or Write from\to memory		Analog		DDR_ VDDQ/DDR_ VDDQX

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
B1	DDR_DQS0_P	I/O	Bi- directional differential output clock signals used to strobe data during READ or Write from\to memory		Analog		DDR_ VDDQ/DDR_ VDDQX
F1	DDR_DQS1_P	I/O	Bi- directional differential output clock signals used to strobe data during READ or Write from\to memory		Analog		DDR_ VDDQ/DDR_ VDDQX
U2	DDR_DQS2_P	I/O	Bi- directional differential output clock signals used to strobe data during READ or Write from\to memory		Analog		DDR_ VDDQ/DDR_ VDDQX
Y1	DDR_DQS3_P	I/O	Bi- directional differential output clock signals used to strobe data during READ or Write from\to memory		Analog		DDR_ VDDQ/DDR_ VDDQX
C2	DDR_DM0	I/O	DDR data mask signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
G3	DDR_DM1	I/O	DDR data mask signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
T1	DDR_DM2	I/O	DDR data mask signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
AA2	DDR_DM3	I/O	DDR data mask signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
H3	DDR_CS0_N	O	Active-low chip select signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
J3	DDR_CS1_N	O	Active-low chip select signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
P3	DDR_CS2	O	Active-low chip select signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
R3	DDR_CS3	O	Active-low chip select signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
J2	DDR_CKE0	O	Active high clock enabling signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
N2	DDR_CKE1	O	Active high clock enabling signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
J1	DDR_CA0	O	Command/ Address signals to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
K3	DDR_CA1	O	Command/ Address signals to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
K2	DDR_CA2	O	Command/ Address signals to the memory	A	Analog		DDR_ VDDQ/DDR_ VDDQX
L3	DDR_CA3	O	Command/ Address signals to the memory	B	Analog		DDR_ VDDQ/DDR_ VDDQX
L2	DDR_CA4	O	Command/ Address signals to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
K1	DDR_CA5	O	Command/ Address signals to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
M1	DDR_CLK_N	O	Differential clock signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
N1	DDR_CLK	O	Differential clock signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
M2	DDR_CAL0	I	Sideband, calibration resistor connection		Analog		DDR_ VDDQ/DDR_ VDDQX
P2	DDR_DATA_RET	I	Sideband, data retention control signal		Analog		DDR_ VDDQ/DDR_ VDDQX

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
N3	DDR_RESET_N	O	Active low reset signal to the memory		Analog		DDR_ VDDQ/DDR_ VDDQX
M3	DDR_ATB0	I/O	Sideband, Analog Test Bus		Analog		
M4	DDR_ATB1	I/O	Sideband, Analog Test Bus		Analog		
Universal Serial Bus Interface							
G6	USB_AVDD_CORE		Analog power supply for USB core		Power		
F6	USB_AVDD_IO		Analog power supply for USB I/O'S		Power		
G8	USB_AVDD_IO_HV		Analog power supply for USB		Power		
E6	USB_VBUS		USB VBUS		Analog		USB_AVDD_ IO/ USB_ AVDD_IO_HV
Ethernet Interface							
Not currently supported, if you wish to use this feature , please contact your Hailo support.							
L21	ETH_RGMII_TXD0	O	Transmit data signal to PHY	Drive 0	LVCMOS		VDDIO
K21	ETH_RGMII_TXD1	O	Transmit data signal to PHY	Drive 0	LVCMOS		VDDIO
K20	ETH_RGMII_TXD2	O	Transmit data signal to PHY	Drive 0	LVCMOS		VDDIO
K22	ETH_RGMII_TXD3	O	Transmit data signal to PHY	Drive 0	LVCMOS		VDDIO
L22	ETH_RGMII_TX_ CLK	[1]	Transmit clock signal to PHY	Drive 0	LVCMOS		VDDIO

[1] The IO will output 0 unless the ETH_RGMII_RX_CLK = 1 , then it will be 1. If the RX clock is not connected the value is 0

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
L20	ETH_RGMII_TX_CTL	O	Transmit control signal to PHY	Drive 0	LVCMOS		VDDIO
N21	ETH_RGMII_RXD0	I	Receive data signal from PHY	PD	LVCMOS	Yes	VDDIO
M21	ETH_RGMII_RXD1	I	Receive data signal from PHY	PD	LVCMOS	Yes	VDDIO
M20	ETH_RGMII_RXD2	I	Receive data signal from PHY	PD	LVCMOS	Yes	VDDIO
M22	ETH_RGMII_RXD3	I	Receive data signal from PHY	PD	LVCMOS	Yes	VDDIO
N22	ETH_RGMII_RX_CLK	I	Receive clock signal from PHY	PD	LVCMOS	Yes	VDDIO
N20	ETH_RGMII_RX_CTL	I	Receive control signal from PHY	PD	LVCMOS	Yes	VDDIO
N19	ETH_MDC	O	Management interface clock	Drive 0	LVCMOS		
M19	ETH_MDIO	I	Management interface data input output	PU	LVCMOS	Yes	VDDIO

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
SPI Interface							
G22	SPI_RESET	O	Flash reset out	Drive 1	LVCMOS		VDDIO
F21	SPI_CS0_N	O	Flash chip select, active low	Drive 1	LVCMOS		VDDIO
G21	SPI_CS1_N	O	Flash chip select, active low	Drive 1	LVCMOS		VDDIO
Pin multiplexed with GPIOs	SPI_CS2_N	O	Flash chip select, active low	Drive 1	LVCMOS		VDDIO
Pin multiplexed with GPIOs	SPI_CS3_N	O	Flash chip select, active low	Drive 1	LVCMOS		VDDIO
D22	SPI_DQ0	I	Flash data in/out	PU	LVCMOS		VDDIO
E22	SPI_DQ1	I	Flash data in/out	PU	LVCMOS		VDDIO
D21	SPI_DQ2	I	Flash data in/out	PU	LVCMOS		VDDIO
E21	SPI_DQ3	I	Flash data in/out	PU	LVCMOS		VDDIO
F22	SPI_SCLK	O	Flash clock	Drive 0	LVCMOS		VDDIO

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
Universal Asynchronous Receiver Transmitter (UART) Interface							
G20	UART0_RXD	I	UART receive data	PD	LVCMOS	Yes	VDDIO
G19	UART1_RXD	I	UART receive data	PD	LVCMOS	Yes	VDDIO
F20	UART0_TXD	O	UART transmit data	PD	LVCMOS		VDDIO
F19	UART1_TXD	O	UART transmit data	Drive 1	LVCMOS		VDDIO
Pin multiplexed with GPIOs	UART[2:3]_RXD	I	UART receive data	PD	LVCMOS		VDDIO
Pin multiplexed with GPIOs	UART[2:3]_TXD	O	UART transmit data	Drive 1	LVCMOS		VDDIO
Pin multiplexed with GPIOs	UART[0:3]_CTS	I	UART flow control, clear to send				
Pin multiplexed with GPIOs	UART[0:3]_RTS	O	UART flow control, request to send				
Inter-Integrated Circuit (I2C) Interface							
D16	I2C0_SDA	I	I2C0 serial data	PU	LVCMOS		VDDIO
B16	I2C1_SDA	I	I2C1 serial data	PU	LVCMOS		VDDIO
C16	I2C0_SCL	I	I2C0 clock	PU	LVCMOS		VDDIO
A16	I2C1_SCL	I	I2C1 clock	PU	LVCMOS		VDDIO
Pin multiplexed with GPIOs	I2C[0:3]_ CURRENT_SRC_EN	O	Fast mode I2C pin				
Pin multiplexed with GPIOs	I2C[2:3]_SDA	I/O	I2C[2-3] serial data				
Pin multiplexed with GPIOs	I2C[2:3]_SCL	O	I2C[2-3] clock				
Reset and Clock							
E20	RESET_N	I	Chip reset, active low	PD	LVCMOS	Yes	VDDIO
H22	OSC_XOUT	O	Crystal out				

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
J22	OSC_XIN	I	Crystal in				
JTAG							
B21	JTAG_TDI	I	JTAG data input	PU	LVCMOS		VDDIO
C21	JTAG_TDO	O	JTAG data output	Drive Low PD	LVCMOS		VDDIO
B22	JTAG_TMS	I	JTAG mode select	PU	LVCMOS		VDDIO
A21	JTAG_TCK	I	JTAG clock	PD	LVCMOS		VDDIO
C22	JTAG_TRSTN	I	JTAG reset. Active low	PD	LVCMOS	Yes	VDDIO
GPIO							
P18	GPIO_0	O	General configurable pins See 1.1. Pin Multiplex Specifications	Drive clk	LVCMOS		VDDIO
P19	GPIO_1	O	"	Drive clk	LVCMOS		VDDIO
P20	GPIO_2	O	"	Drive 1	LVCMOS		VDDIO
P21	GPIO_3	O	"	Drive 0	LVCMOS		VDDIO
P22	GPIO_4	O	"	Drive 0	LVCMOS		VDDIO
R22	GPIO_5	O	"	Drive 1	LVCMOS		VDDIO
R21	GPIO_6	I	"	PD	LVCMOS		VDDIO
R20	GPIO_7	O	"	Drive 0	LVCMOS		VDDIO
R19	GPIO_8	I	"	PD	LVCMOS		VDDIO
R18	GPIO_9	I	"	PD	LVCMOS		VDDIO
T18	GPIO_10	I	"	PD	LVCMOS		VDDIO

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
T19	GPIO_11	I	"	PD	LVCMOS		VDDIO
T20	GPIO_12	O	"	Drive 0	LVCMOS		VDDIO
T21	GPIO_13	I	"	PD	LVCMOS		VDDIO
T22	GPIO_14	I	"	PD	LVCMOS		VDDIO
U22	GPIO_15	O	"	Drive 0	LVCMOS		VDDIO
U21	GPIO_16	I	"	PD	LVCMOS		VDDIO
U20	GPIO_17	I	"	PD	LVCMOS		VDDIO
U19	GPIO_18	I	"	PD	LVCMOS		VDDIO
U18	GPIO_19	I	"	PD	LVCMOS		VDDIO
V18	GPIO_20	I	"	PD	LVCMOS		VDDIO
V19	GPIO_21	I	"	PD	LVCMOS		VDDIO
V20	GPIO_22	I	"	PD	LVCMOS		VDDIO
V21	GPIO_23	I	"	PD	LVCMOS		VDDIO
V22	GPIO_24	I	"	PD	LVCMOS		VDDIO
W22	GPIO_25	O	"	Drive 0	LVCMOS		VDDIO
W21	GPIO_26	O	"	Drive 0	LVCMOS		VDDIO
W20	GPIO_27	O	"	Drive 0	LVCMOS		VDDIO
W19	GPIO_28	O	"	Drive 0	LVCMOS		VDDIO
Y20	GPIO_29	I	"	PD	LVCMOS		VDDIO
Y21	GPIO_30	I	"	PD	LVCMOS		VDDIO
Y22	GPIO_31	O	"	Drive 0	LVCMOS		VDDIO

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger	I/O Voltage
CPU Management							
Pin multiplexed with GPIOs	CPU_TRACE_CLOCK	O	CPU clock out				
Pin multiplexed with GPIOs	CPU_DATA[0-3]	O	CPU trace data out				
Miscellaneous							
H20	SAFETY_ERROR_N	O	Safety error pin	Drive 0	LVCMOS		VDDIO
J20	SAFETY_FATAL_N	O	Safety fatal pin will be asserted after Software Initialization, and de-asserted if a fatal safety event will be detected by the SoC. The pin can also be used as an indication for SoC reset, upon reset, the pin will be de-asserted.	Drive 0	LVCMOS		VDDIO
H19, J19, K19	RSVD						
D17	IO_BS0						

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2.3. Pin Multiplex Specifications

This section describes the possible multiplex configurations available for Hailo-10H GPIOs.
Each of the 32 GPIOs has up to nine options.

Important: Each group of pins can only be set to the same option.

- Option0 – pads_pinmux_mode[3:0] = [0000]
- Option1 – pads_pinmux_mode[3:0] = [0001]
- Option2 – pads_pinmux_mode[3:0] = [0010]
- Option3 – pads_pinmux_mode[3:0] = [0011]
- Option4 – pads_pinmux_mode[3:0] = [0100]
- Option5 – pads_pinmux_mode[3:0] = [0101]
- Option6 – pads_pinmux_mode[3:0] = [0110]
- Option7 – pads_pinmux_mode[3:0] = [0111]
- Option8 – pads_pinmux_mode[3:0] = [1000]
- Option9 – pads_pinmux_mode[3:0] = [1001]

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2.3.1. GPIO Group [0-1]

The multiplex options for GPIO[0] and GPIO[1] are listed in Table 5

Table 5. GPIO Group [0-1] multiplex options

GPIO	Option0	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO0	INITIAL_ DEBUG_BUS [0]	RESERVED	GPIO[0]	I2C0_ CURRENT_ SRC_EN	SPI_CS[2]	RESERVED	Safety_out0	RESERVED	UART2_TXD	I2C2_ CURRENT_ SRC_EN
GPIO1	INITIAL_ DEBUG_BUS [1]	RESERVED	GPIO[1]	I2C1_ CURRENT_ SRC_EN	SPI_CS[3]	RESERVED	Safety_out0	RESERVED	UART3_TXD	I2C3_ CURRENT_ SRC_EN

2.3.2. GPIO Group [2-3]

The multiplex options for GPIO[2] and GPIO[3] are listed in Table 6.

Table 6. GPIO Group [2-3] multiplex options

GPIO	Option0	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO2	INITIAL_ DEBUG_BUS [2]	RESERVED	GPIO[2]	I2C0_ CURRENT_ SRC_EN	RESERVED	RESERVED	Safety_out0	RESERVED	UART2_TXD	I2C2_ CURRENT_ SRC_EN
GPIO3	INITIAL_ DEBUG_BUS [3]	RESERVED	GPIO[3]	I2C1_ CURRENT_ SRC_EN	RESERVED	RESERVED	Safety_out1	RESERVED	UART3_TXD	I2C3_ CURRENT_ SRC_EN

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2.3.3. GPIO Group [4-5]

The multiplex options for GPIO[4] and GPIO[5] are listed in Table 7

Table 7. GPIO Group [4-5] multiplex options

GPIO	Option0	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO4	INITIAL_ DEBUG_BUS [4]	RESERVED	GPIO[4]	GPIO[4]	GPIO[4]	RESERVED	Safety_out0	RESERVED	UART2_TXD	I2C2_ CURRENT_ SRC_EN
GPIO5	INITIAL_ DEBUG_BUS [5]	RESERVED	GPIO[5]	I2C3_ CURRENT_ SRC_EN	I2S_SDO1_out	RESERVED	Safety_out1	RESERVED	UART3_TXD	RESERVED

2.3.4. GPIO Group [6-7]

The multiplex options for GPIO[6] and GPIO[7] are listed in Table 8

Table 8. GPIO Group [6-7] multiplex options

GPIO	Option0	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO6	UART1_CTS	RESERVED	GPIO[6]	RESERVED	RESERVED	RESERVED	UART2_RXD	I2C2_SDA	I2C3_SDA	UART3_CTS
GPIO7	UART1_RTS	RESERVED	GPIO[7]	RESERVED	RESERVED	RESERVED	UART3_RXD	I2C2_SCL	I2C3_SCL	UART3_RTS

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2.3.5. GPIO Group [8-15]

The multiplex options for GPIO[8] to GPIO[15] are listed in Table 9

Table 9. GPIO Group [8-15] multiplex options

GPIO	Option0	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO8	GPIO[8]	RESERVED	GPIO[8]	GPIO[8]	RESERVED	GPIO[8]	GPIO[8]	UART2_RXD
GPIO9	RESERVED	RESERVED	GPIO[9]	RESERVED	RESERVED	RESERVED	RESERVED	UART2_TXD
GPIO10	RESERVED	RESERVED	GPIO[10]	RESERVED	RESERVED	RESERVED	RESERVED	UART0_CTS
GPIO11	RESERVED	RESERVED	GPIO[11]	RESERVED	RESERVED	GPIO[11]	RESERVED	UART0_RTS
GPIO12	RESERVED	RESERVED	GPIO[12]	RESERVED	RESERVED	Safety_out1	RESERVED	UART3_RXD
GPIO13	RESERVED	RESERVED	GPIO[13]	I2C1_CURRENT_SRC_EN	RESERVED	GPIO[13]	RESERVED	UART3_TXD
GPIO14	RESERVED	RESERVED	GPIO[14]	GPIO[14]	RESERVED	Safety_out0	RESERVED	GPIO[14]
GPIO15	MPP_mperst_out	RESERVED	GPIO[15]	MPP_mperst_out	RESERVED	MPP_mperst_out	GPIO[15]	MPP_mperst_out

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2.3.6. GPIO Group [16-31]

The multiplex options for GPIO[16] to GPIO[31] are listed in Table 10

Table 10. GPIO Group [16-31] multiplex options

GPIO	Option0	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO16	GPIO[16]	RESERVED	GPIO[16]	GPIO[16]	RESERVED	UART2_RXD	GPIO[16]	RESERVED
GPIO17	GPIO[17]	RESERVED	GPIO[17]	GPIO[17]	RESERVED	UART2_TXD	GPIO[17]	RESERVED
GPIO18	RESERVED	RESERVED	GPIO[18]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
GPIO19	RESERVED	RESERVED	GPIO[19]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
GPIO20	GPIO[20]	RESERVED	GPIO[20]	GPIO[20]	RESERVED	I2C3_SDA	GPIO[20]	RESERVED
GPIO21	GPIO[21]	RESERVED	GPIO[21]	GPIO[21]	RESERVED	I2C3_SCL	GPIO[21]	RESERVED
GPIO22	GPIO[22]	RESERVED	GPIO[22]	I2C2_SDA	RESERVED	I2C2_SDA	GPIO[22]	RESERVED
GPIO23	GPIO[23]	RESERVED	GPIO[23]	I2C2_SCL	RESERVED	I2C2_SCL	GPIO[23]	RESERVED
GPIO24	RESERVED	RESERVED	GPIO[24]	I2C2_CURRENT_SRC_EN	RESERVED	I2C0_CURRENT_SRC_EN	GPIO[24]	RESERVED
GPIO25	I2C0_CURRENT_SRC_EN	RESERVED	GPIO[25]	I2C0_CURRENT_SRC_EN	RESERVED	I2C1_CURRENT_SRC_EN	I2C0_CURRENT_SRC_EN	RESERVED
GPIO26	I2C1_CURRENT_SRC_EN	RESERVED	GPIO[26]	I2C1_CURRENT_SRC_EN	RESERVED	UART1_CTS	I2C1_CURRENT_SRC_EN	RESERVED
GPIO27	RESERVED	RESERVED	GPIO[27]	GPIO[27]	RESERVED	UART1_RTS	GPIO[27]	CPU_TRACE_CLK
GPIO28	RESERVED	RESERVED	GPIO[28]	GPIO[28]	RESERVED	UART2_CTS	GPIO[28]	CPU_TRACE_DATA[0]

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GPIO	Option0	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO29	GPIO[29]	RESERVED	GPIO[29]	GPIO[29]	RESERVED	UART2_RTS	GPIO[29]	CPU_TRACE_DATA[1]
GPIO30	UART0_CTS	RESERVED	GPIO[30]	UART0_CTS	RESERVED	UART0_CTS	GPIO[30]	CPU_TRACE_DATA[2]
GPIO31	UART0_RTS	RESERVED	GPIO[31]	UART0_RTS	RESERVED	UART0_RTS	GPIO[31]	CPU_TRACE_DATA[3]

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2.4. Initial Debug Bus

During boot, GPIO[0:5] serves as “initial debug bus” signals and is actively driven by Hailo-10H and therefore may toggle or change state during this time. System design must take into consideration this behavior and make provisions to handle it by either gating these signals during boot or ensuring that the devices attached to these GPIO’s can tolerate this behavior

Table 11 below provides a description and behavior of the INITIAL_DEBUG_BUS of GPIO[0:5] during boot.

Table 11. GPIO [0:5} signal behavior during boot

GPIO Signal	Expected Behavior During Boot
0	25MHz clock
1	PCIe boot - starts LOW and then switches to 25MHz clock by HW and then switch to 200MHz clock by BootRom code Flash boot - starts LOW and then switches to 25MHz clock. *In some flows gated by ROM after flow is passed.
2	Starts Low, asserts to High, and then according to the ‘life cycle state’ of the chip
3	Starts Low, asserts to High, and then according to the ‘life cycle state’ of the chip
4	Starts LOW and assert to HIGH
5	Starts HIGH and negate to LOW

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3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 12 and Table 13 may cause permanent damage to the device and affect device reliability. These are stress ratings only and functional operation of the device at these conditions is not implied.

3.1.1. Power Rails

Table 12 provides the absolute maximum ratings of the power rails.

Table 12. Absolute maximum power rail ratings

Supply Name	Description	Min	Max	Unit
Digital Power Rails				
VDD	Digital CMOS supply of SoC	-0.5	1.05	V
VDDIO	IO banks	-0.5	2.5	V
MPP (Multi-Protocol PHY) Analog Power Rails				
MPP_AVDD_D	Analog power for non-high-speed clock and digital functions	-0.5	1.05	V
MPP_AVDD_C	Clean analog power for high-speed clock applications	-0.5	1.05	V
MPP_AVDD_H	High voltage power for the bias and parts of the PLL	-0.5	2.5	V
USB PHY Analog Power Rails				
USB_AVDD_CORE	USB core	-0.5	1.05	V
USB_AVDD_IO	USB IO	-0.5	2.5	V
USB_AVDD_IO_HV	Clean analog power supply for USB IO	-0.5	3.63	V
DDR Power Rails				
DDR_VDD	DDR Core Supply Voltage	-0.5	1.05	V
DDR_VDDQ	DDR I/O driver supply	-0.5	1.2	V
DDR_VDDQX	DDR I/O pre-driver supply	-0.5	1.2	V
DDR_VDDPLL	DDR PLL analog supply	-0.5	1.05	V
DDR_VDDQ_CK	IO power for DDR Memory Clock Bit (MCB) macro	-0.5	1.2	V
Miscellaneous				
PLL_VDDA	PLL analog power rail of the MAIN_PLL, AP_PLL and CORE_PLL	-0.5	1.05	V
DDR_PLL_VDDA	PLL analog power rail of the internal DDR PLL	-0.5	1.05	V
FUSE_VQPS	Factory use only - connect to GND	-	-	V
AVDD_TS	Temperature sensor analog power rail	-0.5	2.5	V
AVDD_VM	Voltage sensor analog power rail	-0.5	2.5	V
Input voltage applied to digital IOs	Input Low Voltage	-0.5	2.5	V

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Supply Name	Description	Min	Max	Unit
V_ESD (HBM)	Electrostatic discharge voltage (Human Body Model)	1000		V
V_ESD (CDM)	Electrostatic discharge voltage (Charged Device Model)	500		V
Latch UP (LU)	Class II of JESD78E immunity level	A[1]		V

3.1.2. Thermal Ratings

Table 13 provides the storage and maximum junction temperature values.

Table 13. Absolute maximum thermal ratings

Parameter	Description	Value	Unit
T_Storage	Storage temperature	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

3.1.3. Thermal Design Power

The TDP (Thermal Design Power) measured in watts, is the power consumption under the maximum theoretical load to which a system is designed. This ensures operation to published specs under the maximum theoretical workload.

The TDP for Hailo 10H is 8 Watts.

3.2. Recommended Operating Conditions

Table 14 describes the recommended operating conditions for power rails, clocks, and ambient temperature.

Table 14. Hailo-10H operating ranges

Supply Name	Description	Min	Nom	Max	Unit
Digital Domain Power Rails					
VDD	Digital CMOS supply of SoC	0.76	0.8	0.88	V
VDDIO	Digital Power Rail for IO banks	1.62	1.8	1.98	V

[1] Immunity level A: Pass the ±100mA and 1.5xVdd or MSV

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Supply Name	Description	Min	Nom	Max	Unit
PCIe PHY Analog Power Rails					
MPP_AVDD_D	Analog power for non-high-speed clock and digital functions	0.76	0.8	0.88	V
MPP_AVDD_C	Clean analog power for high-speed clock applications	0.76	0.8	0.88	V
MPP_AVDD_H	High voltage power for the bias and parts of the PLL	1.08	1.8	1.98	V
USB PHY Analog Power Rails					
USB_AVDD_CORE	Analog power supply for the USB core	0.76	0.8	0.88	V
USB_AVDD_IO	Analog power supply for the USB's IO	1.62	1.8	1.98	V
USB_AVDD_IO_HV	Clean analog power supply for USB's IO	2.97	3.3	3.63	V
DDR Power Rails					
DDR_VDD	DDR Core Supply Voltage	0.72	0.8	0.88	V
DDR_VDDQ	DDR I/O driver supply	1.06[1] or 0.57[2]	1.1[1] or 0.6[2]	1.17[1] or 0.65[2]	V
DDR_ VDDQX	DDR I/O pre-driver supply	1.06	1.1	1.17	V
DDR_ VDDPLL	Analog Core Supply	0.72	0.8	0.88	V
DDR_ VDDQ_CK	IO power for DDR Memory Clock Bit (MCB) macro	Same as DDR_VDDQ			V

[1]When LPDDR4 device is being used
[2]When LPDDR4X device is being used

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Supply Name	Description	Min	Nom	Max	Unit
Miscellaneous					
PLL_VDDA	PLL analog power rail of the MAIN_PLL, AP_PLL and CORE_PLL	0.76	0.8	0.88	V
DDR_PLL_ VDDA	PLL analog power rail of the internal DDR PLL	0.76	0.8	0.88	V
FUSE_VQPS	Factory use only -connect to GND	-	-	-	V
AVDD_TS	Temperature sensor analog power rail	1.62	1.8	1.98	V
AVDD_VM	Voltage sensor analog power rail	1.62	1.8	1.98	V
External Clocks					
Oscillator [1]	Frequency	25±100PPM			MHz
	Duty Cycle	40	50	60	%
Crystal[2]	Frequency	25 +/- 30 PPM			MHz
Ambient Operating Temperature					
T_A	Industrial grade	-40		85	^{o}C

[1] Connected to OSC_XIN clock pin, must receive a square wave clock signal (oscillator output clock signal)

[2]Connected to OSC_XIN and OSC_XOUT pin, must receive a Sine wave

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3.3. Power-up Sequence

The power-up sequence should follow these guidelines:

1. Initial state: RESET_N pin is asserted (held low).
2. VDDIO rises to 1.8V. Slew rate should be less than 18V/ms.
3. The VDD rises to 0.8V. VDD must hold VDD<VDDIO-0.3V. Slew rate of VDD should be less than 18V/ms.
4. DDR_PLL_VDDA and PLL_VDDA should rise with VDD, and be powered from VDD power regulator with filtering.
5. After VDD is stable
   a. Power-up DDR_VDD, DDR_VDDPLL, DDR_VDDQX and DDR_VDDQ.
      - DDR_VDD and DDR_VDDPLL can short with VDD as long as VDD noise target is met.

   DDR_VDD and DDR_VDDPLL should be powered up earlier than DDR_VDDQX and DDR_VDDQ.

   DDR_VDDQX must rise at **the** same time or earlier than DDR_VDDQ, and DDR_VDDQX must always be greater than or equal to DDR_VDDQ.

   b. FUSE_VQPS should rise later than VDD and power off before VDD is ramped down.
6. Power-up MPP_AVDD_D, MPP_AVDD_C, and MPP_AVDD_H in any order. There are no timing limitations (minimum or maximum) between powering-up multiple power supplies.
   - MPP_AVDD_D, MPP_AVDD_C can be powered from VDD power regulator as long as **the** noise target is met.
   - MPP_AVDD_H can power prior to MPP_AVDD_D and MPP_AVDD_C
7. There is no particular voltage dependency for USB_ AVDD_CORE, VDD, USB_AVDD_IO and USB_ AVDD_IO_HV supplies.

   USB_AVDD_CORE, USB_AVDD_IO, USB_AVDD_IO_HV can be in any order, there is no specific ramp-up sequence between them and each supply ramp-up is independent of each other.

   Time of ramp up for all supply must be between 10µs to 5ms.

   Between the supplied and VBUS – there is no specific ramp up, and VBUS can be present when there are either supplies or no supplies provided to the USB interface
8. Enable reference clock after VDDIO is stable
9. De-assert RESET_N after clock is stable.

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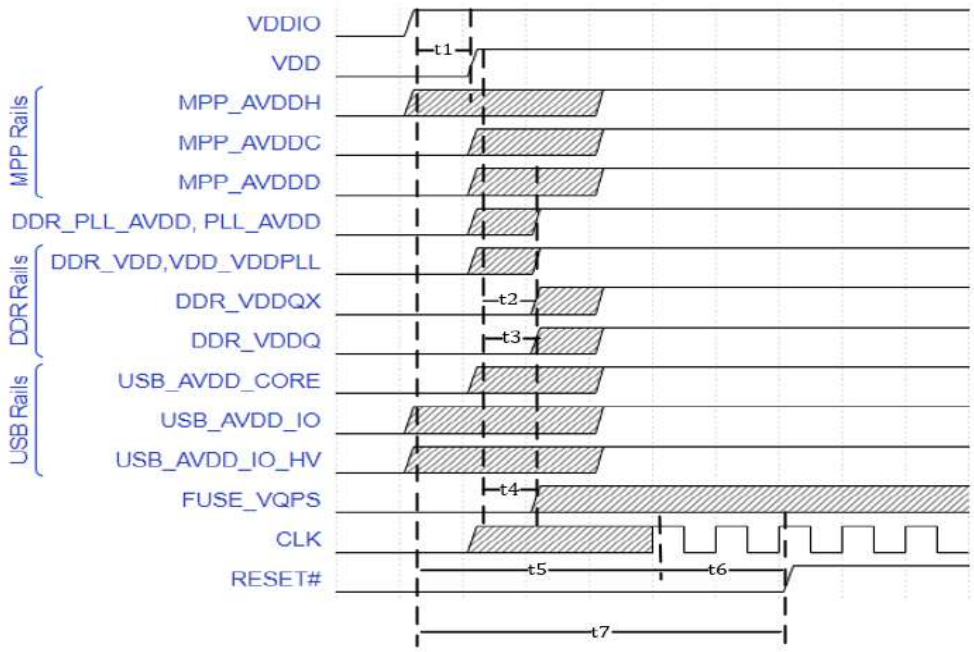


Figure 4. Power-up sequence

Table 15. Power-up Sequence Timing Requirements

	Description	Min	Nom	Max	Unit	Comment
T1	VDDIO to VDD	1	-	-	us	
T2	DDR_VDD to DDR_VDDQX	1	-	-	us	
T3	DDR_VDD to DDR_VDDQ	1	-	-	us	
T4	VDD to FUSE_VQPS	1	-	-	us	
T5	VDDIO to Stable Clock	1	-	-	us	
T6	Stable CLK to RESET_N de-assertion	100	-	-	us	
T7	VDDIO to RESET_N de-assertion	1	-	70	ms	For non-PCIE implementation
		1	-	PERST#	ms	For PCIE implementation

Notes: [1], [2]

[1] Requirement derived from PCI Express® Specification Rev 3.0, "2.6.2. AC Specifications":

Symbol	Parameter	Min	Max	Units	Notes
T_{PVPERL}	Power stable to PERST# inactive	100		ms	1

[2] Refer to the respective additional timing requirements where relevant within this datasheet.

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3.4. Power Consumption

3.4.1. Maximum Supply Current

The maximum current that can be drawn from each power rail is application dependent. The measurements in Table 16 Maximum supply current were made during device characterization and represent worst-case results across all PVT corners. The numbers are provided here only as general guidelines for power supply design.
***NOTE:** The Max Current data below is subject to confirmation.

Table 16. Maximum supply current

Supply Name	*Max Current	Unit
VDD[1]	10	A
VDDIO[2]	0.3	A
MPP_AVDD_D	255	mA
MPP_AVDD_C	TBD	mA
MPP_AVDD_H	TBD	uA
USB_AVDD_CORE	9	mA
USB_AVDD_IO	10	mA
USB_AVDD_IO_HV	1	mA
PLL_VDDA	10	mA
DDR_PLL_VDDA	4	mA
DDR_VDD	1400	mA
DDR_VDDQ	165	mA
DDR_VDDQX	5	mA
DDR_VDDPLL	55	mA
DDR_VDDQ_CK	130	mA
AVDD_TS	0.5	mA
AVDD_VS	0.3	mA

3.4.2. Power Consumption in Selected Test Cases

TBD

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[1] The maximum current assumes heavy compute networks, for lowering the values, if needed, please evaluate the specific neural model and SoC integration for the specific network and add an adequate margin to cover all PVT corners and current spikes.

[2] $VDDIO[V] \cdot \sum_{IO_i} \left(C_i[F] \cdot \frac{1}{2} \cdot f_{switching}[Hz] \right)$ Each IO_i drives a capacitance C_i[F] and is switched from 1 to 0 and vice versa at a frequency of 0.5f[Hz]. Add C_i[F]x0.5f[Hz] of all the IOs and multiply this sum by the VDDIO [V] voltage rail to obtain the VDDIO current consumption
I_VDDIO[A].

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3.4.3. Power Modes

3.4.3.1. Thermal Throttling

The thermal throttling mechanism's main purpose is to keep the Hailo-10HVPU from overheating during operation and exceeding absolute maximum ratings. The throttling mechanism is enabled by default but can be deactivated by the system integrator.

While it operates, the temperature sensors embedded in the chip silicon are configured to interrupt the SCU (ARM Cortex M4) executing Hailo-10H FW when a temperature threshold is crossed.

When a temperature threshold cross is detected, Hailo- 10H FW starts to reduce the clock frequency of the NN-core , which should reduce the dynamic power of the chip and expectantly it's junction temperature.

The thermal throttling has seven throttling levels with corresponding threshold values:

- Full performance
- Light
- Medium
- Heavy
- Severe
- Stream off
- Shut down

The higher the monitored temperature, the heavier the throttling level and therefore the clock frequency of the NN-core will be further reduced.

In the case of an event indicating the monitored temperature is cooling down, the Hailo-10H FW will increase the NN-core frequency, and the temperature will pass a set of hysteresis thresholds, recovering the performance degradation.

When the monitored temperature exceeds the last threshold, the SCU (ARM Cortex M4) is interrupted again, and in this case, the Hailo-10H FW will force system shut down, this mechanism is an 'always-on mechanism'.

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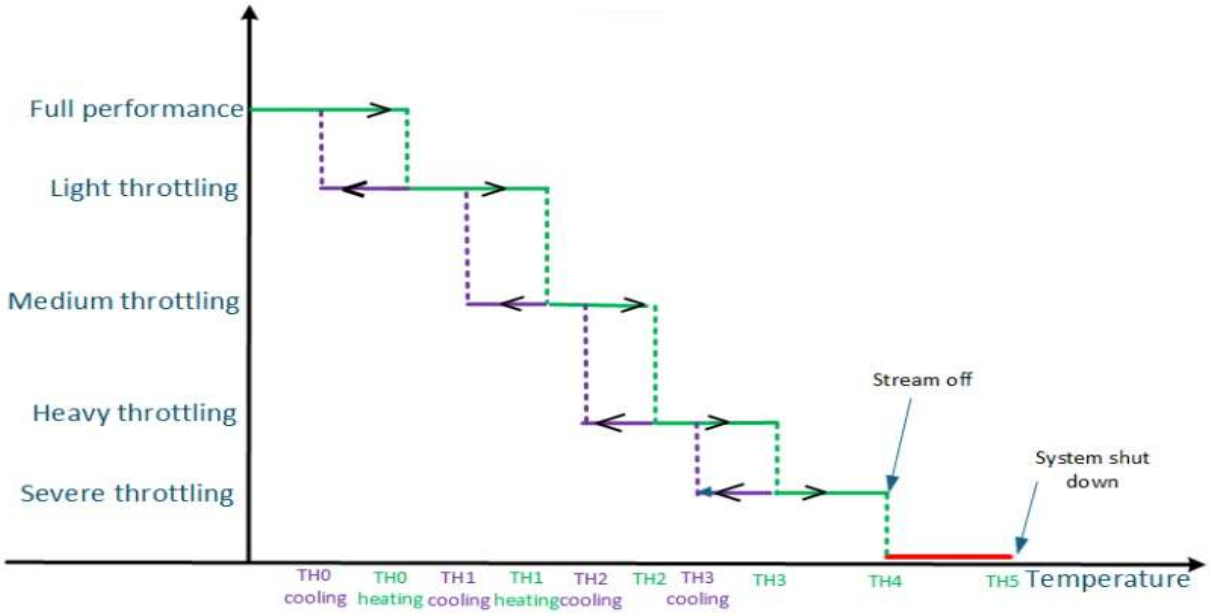


Figure 5. Increasing frequency of thermal throttling decreases chip temperature

Table 17. below shows the sample temperature and temperature hysteresis values at different throttling levels.

Table 17. Hysteresis between heating and cooling for each of the threshold crossings

Throttling Level	Entry TH [C]	Recovery TH [C]	'Core' clk [MHz] (sourced by the core PLL)
Full performance			600
Light	80 (TH0_heating)	75 (TH0_cooling)	525
Medium	105 (TH1_heating)	100 (TH1_cooling)	450
Heavy	110 (TH2_heating)	107 (TH2_cooling	300
Severe	115 (TH3_heating)	112 (TH3_cooling)	150
Stream off	119 (TH4_heating)	User	n/a
Shut down	122 (TH5_heating)	na	n/a

3.5. Digital I/O DC Characteristics

Table 18 describes the DC characteristics of the following failsafe digital pads as characterized across all PVT corners.

- GPIO_0
- GPIO_1
- HRESETN
- PCIE_PERST

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- PCIE_CLKREQ
- PCIE_WAKE

Table 18. Failsafe digital pin DC characteristics

Symbol	Parameter	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.35*VDDIO	V
V_{IH}	Input High Voltage	0.65*VDDIO		1.98	V
V_T	Threshold Point	0.91	1	1.13	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.97	1.09	1.2	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.75	0.86	0.97	V
V_{TPU}	Threshold point with Pull-Up Resistor Enabled	0.82	0.95	1.07	V
V_{TPD}	Threshold point with Pull-Down Resistor Enabled	0.91	1.01	1.14	V
V_{T+PU}	Schmitt Trigger Low to High Threshold Point with Pull-Up Resistor Enabled	0.87	1	1.13	V
V_{T-PU}	Schmitt Trigger High to Low Threshold Point with Pull-Up Resistor Enabled	0.69	0.8	0.92	V
V_{T+PD}	Schmitt Trigger Low to High Threshold Point with Pull-Down Resistor Enabled	0.98	1.09	1.22	V
V_{T-PD}	Schmitt Trigger High to Low Threshold Point with Pull-Down Resistor Enabled	0.75	0.86	0.98	V
I_L	Input Leakage Current @ Vi=1.8V or 0V			+/-10	uA
I_{OZ}	Tri-State Output Leakage Current @ Vi=1.8V or 0V			+/-10	uA
R_{PU}	Pull-Up Resistor	31	46	84	KΩ
R_{PD}	Pull-Down Resistor	31	44	71	KΩ
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
C	Output/Input capacitance	-	1.05	-	pF

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Table 19 describes the DC characteristics of the regular IOs pins, as characterized across all PVT corners. It applies to all digital IOs except for the failsafe list mentioned above in Table 18

Table 19. Regular GPIOs DC characteristics

Symbol	Parameter	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.35*VDDIO	V
V_{IH}	Input High Voltage	0.65*VDDIO		1.98	V
V_{T}	Threshold Point	0.82	0.92	1	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.98	1.1	1.21	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.74	0.82	0.9	V
V_{TPU}	Threshold point with Pull-Up Resistor Enabled	0.82	0.91	1	V
V_{TPD}	Threshold point with Pull-Down Resistor Enabled	0.83	0.93	1.02	V
V_{T+PU}	Schmitt Trigger Low to High Threshold Point with Pull-Up Resistor Enabled	0.97	1.09	1.2	V
V_{T-PU}	Schmitt Trigger High to Low Threshold Point with Pull-Up Resistor Enabled	0.73	0.81	0.89	V
V_{T+PD}	Schmitt Trigger Low to High Threshold Point with Pull-Down Resistor Enabled	0.99	1.11	1.22	V
V_{T-PD}	Schmitt Trigger High to Low Threshold Point with Pull-Down Resistor Enabled	0.75	0.83	0.91	V
I_{L}	Input Leakage Current @ Vi=1.8V or 0V			+/-10	uA
I_{OZ}	Tri-State Output Leakage Current @ Vi=1.8V or 0V			+/-10	uA
R_{PU}	Pull-Up Resistor	17	24	40	KΩ
R_{PD}	Pull-Down Resistor	17	23	36	KΩ
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
C	Output/Input capacitance for all other pads	-	0.88	-	pF

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3.6. DDR Characteristics

3.6.1. Electrical Operating Conditions

The following tables describe the electrical operating conditions for the LPDDR4/LPDDR4X in the different DDR memory interfaces.

Table 20. Electrical operating conditions for LPDDR4

Mode	Voltage Domain	Min	Typical	Max
LPDDR4	DDR_VDD, DDR_VDDPLL	0.72V	0.80V	0.88V
	DDR_VDDQ, DDR_VDDQ_CK	1.06V	1.10V	1.17V
	DDR_VDDQX	1.06V	1.10V	1.17V

Table 21. Electrical operating conditions for LPDDR4X

Mode	Voltage Domain	Min	Typical	Max
LPDDR4X	DDR_VDD, DDR_VDDPLL	0.72V	0.80V	0.88V
	DDR_VDDQ, DDR_VDDQ_CK	0.57V	0.60V	0.65V
	DDR_VDDQX	1.06V	1.10V	1.17V

3.6.2. TT Clock-DQS Delay at Nominal Voltage and Temperature

Figure 6 below shows the DQS skew with respect to clock for three parts at VDD Core 0.80V, IO-Voltage 0.60V and temperature 25°C.

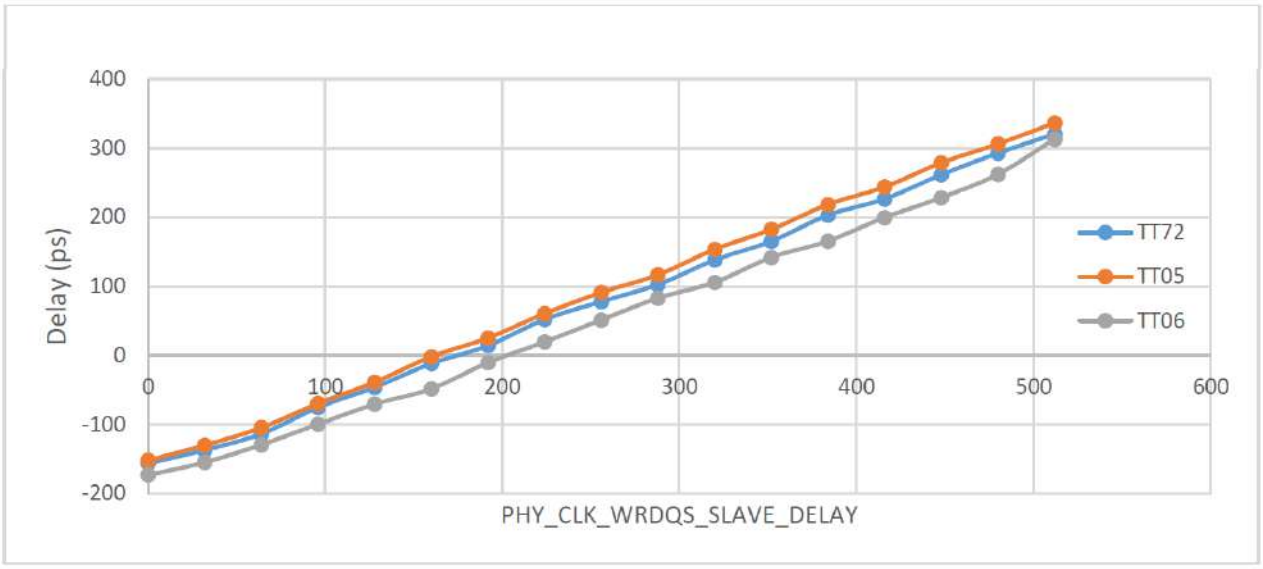


Figure 6. CLK-DQS Delay for TT @Nominal VT

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3.7. USB 3.1 Characteristics

USB 3.1 uses the same characteristics as the PCIe Multiple Protocol PHY please refer to Section 3.7.

3.8. PCIe Characteristics

The following tables describe the Multiple Protocol PHY characteristics as characterized across all PVT corners.

PCIe Characteristics (DC and AC) tables will appear in a future revision.

Table 22. PCIe Gen1 transmitter characteristics

Parameter	Description	PCIe 3.1 Spec Min	PCIe 3.1 Spec Max	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800	1200	876	1130	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	400	1200	489.33	669.19	mV
LTX-SKEW	Lane-to-Lane Output Skew		2.5	-	0.438	ns

Table 23. PCIe Gen2 transmitter characteristics

Parameter	Description	PCIe 3.1 Spec Min	PCIe 3.1 Spec Max	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800	1200	810	1070	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	400	1200	445	625	mV
LTX-SKEW	Lane-to-Lane Output Skew		2	-	0.235	ns

Table 24. PCIe Gen3 transmitter characteristics

Parameter	Description	PCIe 3.1 Spec Min	PCIe 3.1 Spec Max	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800	1300	800	1010	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	400	1300	401	547	mV

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Parameter	Description	PCIe 3.1 Spec Min	PCIe 3.1 Spec Max	Min	Max	Unit
VTX-EIEOS-FS	Minimum voltage swing during EIEOS for full swing signaling	250		262	-	mVPP
VTX-EIEOS-RS	Minimum voltage swing during EIEOS for reduced swing signaling	232		256	-	mVPP
LTX-SKEW	Lane-to-Lane Output Skew		1.5	-	0.438	ns

Table 25. PCIe transmitter data rate independent characteristics

Parameter	Description	PCIe 3.1 Spec Min	PCIe 3.1 Spec Max	Min	Max	Unit
VTX-AC-CM-PP	Tx AC peak-peak common mode voltage		150	-	134	mVPP
VTX-DC-CM	Tx DC peak-peak common mode voltage	0	3.6	0.396	0.404	V
VTX-CM-DC-LINE-DELTA	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	25	2.1	7.2	mV
VTX-IDLE-DIFF-AC-p	Electrical Idle Differential Peak Output Voltage	0	20	8.09	19.98	mV
VTX-IDLE-DIFF-DC	DC Electrical Idle Differential Output Voltage	0	5	0.1	1.4	mV
ZTX-DIFF-DC	DC differential Tx impedance		120	69.2	75.3	Ω

Table 26. PCIe receiver electrical idle detect threshold

Parameter	Description	PCIe 3.1 Spec Min	PCIe 3.1 Spec Max	Min	Max	Unit
VRX-IDLE-DET-DIFF-PP	Electrical Idle Detect threshold	65	175	92	154	mV

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Table 27. PCIe receiver termination characteristics

Parameter	Description	PCIe 3.1 Spec Min	PCIe 3.1 Spec Max	Min	Max	Unit
ZRX-DC	Receiver DC single ended impedance	40	60	49.7	54.9	Ω
ZRX-HIGH-IMP-DC-POS (0-200 mV)	DC input CM input impedance for V≥0 during Reset or power-down	10K		53k	-	Ω
ZRX-HIGH-IMP-DC-POS (> 200 mV)	DC input CM input impedance for V≥0 during Reset or power-down	20K		144k	-	Ω
ZRX-HIGH-IMP-DC-NEG	DC input CM input impedance for V<0 during Reset or power-down	1.0K		4.6k	-	Ω

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3.9. RGMII Timing Characteristics

Not currently supported, if you wish to use this feature , please contact your Hailo support.

Meeting the timing requirements of the RGMII interface, as described here, is crucial for proper operation when interfacing RGMII compliant devices.

Table 28. RGMII Timing Requirements

Parameter	Description	Min	Typical	Max	Unit
T_cyc[1]	Clock cycle duration	7.2	8	8.8	ns
Duty_G [2]	Duty cycle for Gigabit mode	45	50	55	%
Duty_T[2]	Duty cycle for 100T mode	40	50	60	%
TskewT [3]	Data to clock output skew at transmitter	-500	0	500	ps
TskewR[3]	Data to clock input skew at receiver	1	1.8	2.6	ns
Tr / Tf	Rise/Fall time 20-80%	-	-	0.75	ns

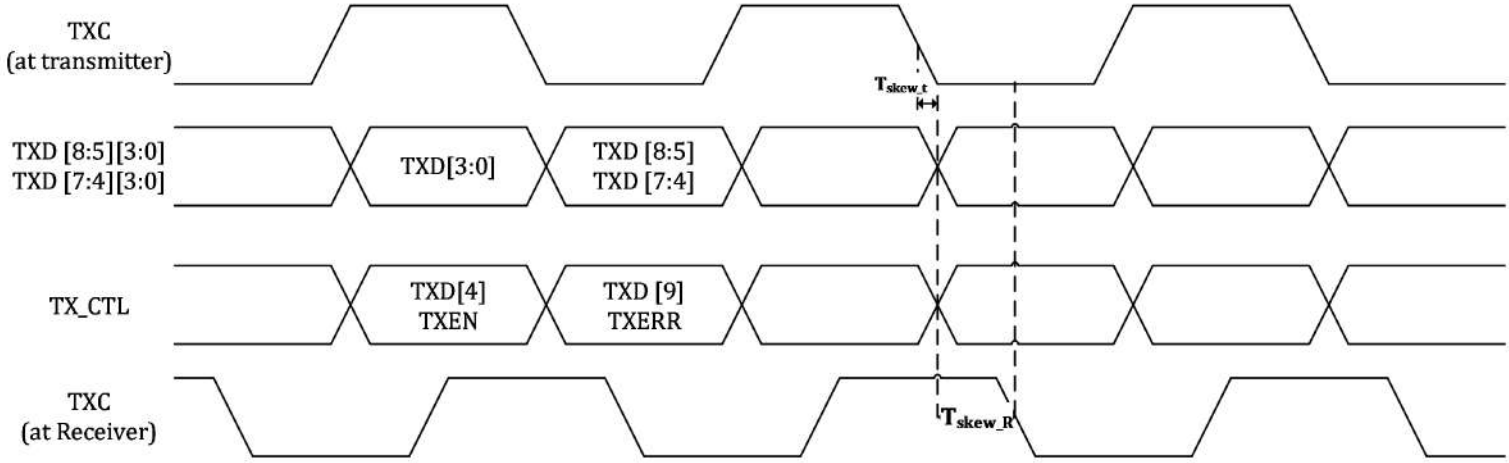


Figure 7. RGMII multiplexing & timing diagram – TX signals

[1] For 100Mbps, Tcyc will scale to 40ns+-4ns.

[2] The duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain on condition that the minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest transitioning speed.

[3] This applies to all versions of RGMII prior to 2.0. This implies that PC board design will require clocks to be routed with an additional trace delay of greater than 1.5ns and less than 2.0ns, to be added to the associated clock signal. For 100Mbps, the maximum value is unspecified.

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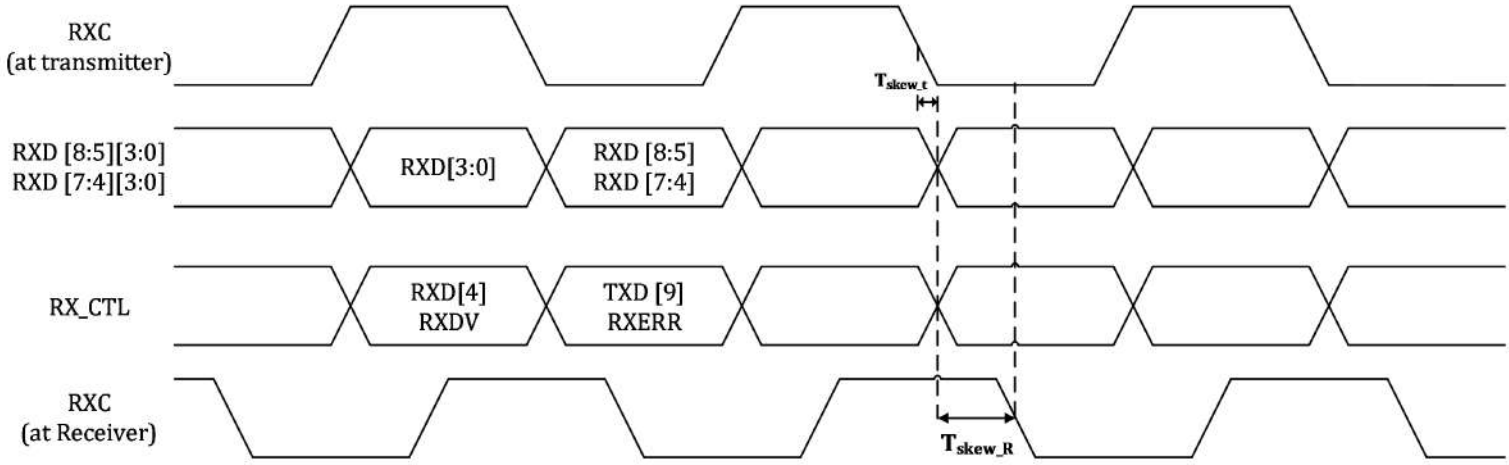


Figure 8. RGMII multiplexing & timing diagram – RX signals

3.10. RMII Timing Characteristics

Not currently supported, if you wish to use this feature , please contact your Hailo support.

Table 29 describes the RMII Timing Characteristics

Table 29 . RMII Timing Characteristics

Parameter	Description	Min	Typical	Max	Unit
T_cyc	Clock cycle duration	18	20	22	ns
Duty_cyc	Duty cycle	45	50	55	%
T_set	Setup time	4	-	-	ns
T_hold	Hold time	2	-	-	ns

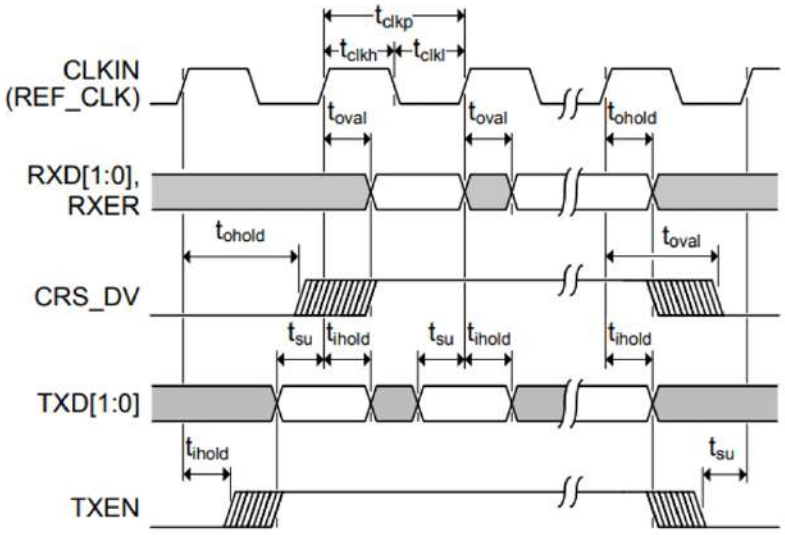


Figure 9. RMII Timing (Ref_CLK In Mode)

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3.11. QSPI Timing Characteristics

Table 30 describes the QSPI Timing Characteristics

Table 30. QSPI Timing Characteristics

Parameter	Description	Min	Typical	Max	Unit
T_cyc	Clock cycle duration	20		160	ns
Duty_cyc	Duty cycle	45	50	55	%
T_set	Setup time	2.8	-	-	ns
T_hold	Hold time	3	-	-	ns

3.12. Reset Timing Characteristics

The NRESET pin should be driven by a Reset signal that meets the following requirements to provide Hailo-10H with a proper Reset pulse:

1. Rise and fall time (measured between 20% and 80% of VDDIO) < 5ns
2. NRESET assertion time (held low) >28us.

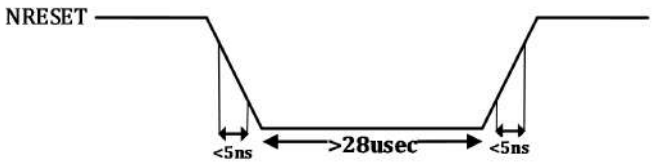


Figure 10. Reset Characteristics

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4. System Modes and Usage

This section describes various system modes and usage scenarios and provides detailed information on these various Hailo-10H subsystems.

See Hailo Software documentation for further descriptions.

4.1. Bootstraps

The Hailo-10H supports boot from flash memory, PCIe or from UART IF.

Hailo-10H has two bootstrap pins, which select the boot-up interface of the M4 MCU.

Note: Since the IF to which this pin is multiplexed to is not functional at this stage, the default pull-down resistor would pull this line down, therefore the signal level is determined by the internal pull-down and the external pull resistor (which is used to select the boot mode), until this signal will be driven from the SoC internals.

Table 31. Bootstrap pin names and functions

Name and Function	Description	Default
bs_io_sel[1:0]– bs_io_sel[0] multiplexed with i2s_sdo[1] **uart0_tx** – bs_io_sel[1] multiplexed with uart0_tx	IO select decoding bs_io_sel[1:0] = 00 – m4 MCU boot from serial (Q)SPI Flash (default) 01 – Boot from UART 10 – Boot from PCIe 11 - Reserved	00

[1] i2s_sdo is the pin function after boot

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4.2. Boot Modes

4.2.1. Boot from PCIe

For PCIe boot, the SoC ROM handles the process with the host platform that runs the Hailo RT PCIe driver. Firmware is then fetched over the PCIe link to boot the device firmware.

4.2.2. Boot from Flash

When this option is selected, ROM code reads the MCU image from an external (Q)SPI Flash device, authenticates it and executes the MCU code, which will in turn fetch the AP bootloader and release the AP reset to start its boot-up process.

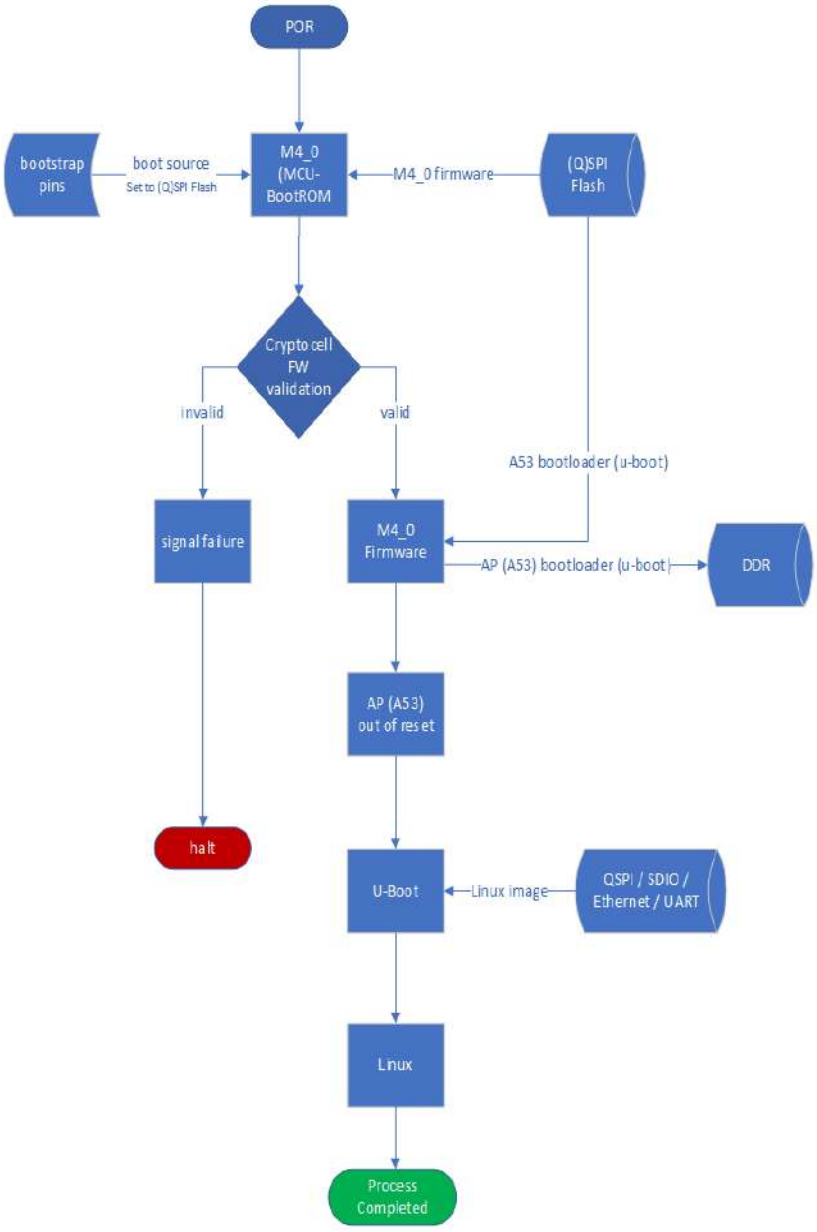


Figure 11. Boot from Flash

Diagram showing the boot from Flash flow, where ROM code reads the MCU image from an external (Q)SPI Flash device.

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4.2.3. Boot from UART

This flow may be considered as a recovery flow, or as a production flow for initial Flash fusing. It is based on a simple proprietary data transfer protocol over the UART1 interface, which enables a device with empty flash to receive the MCU image over a UART interface, write the MCU FW to the flash, and then boot the device from the newly programmed flash.

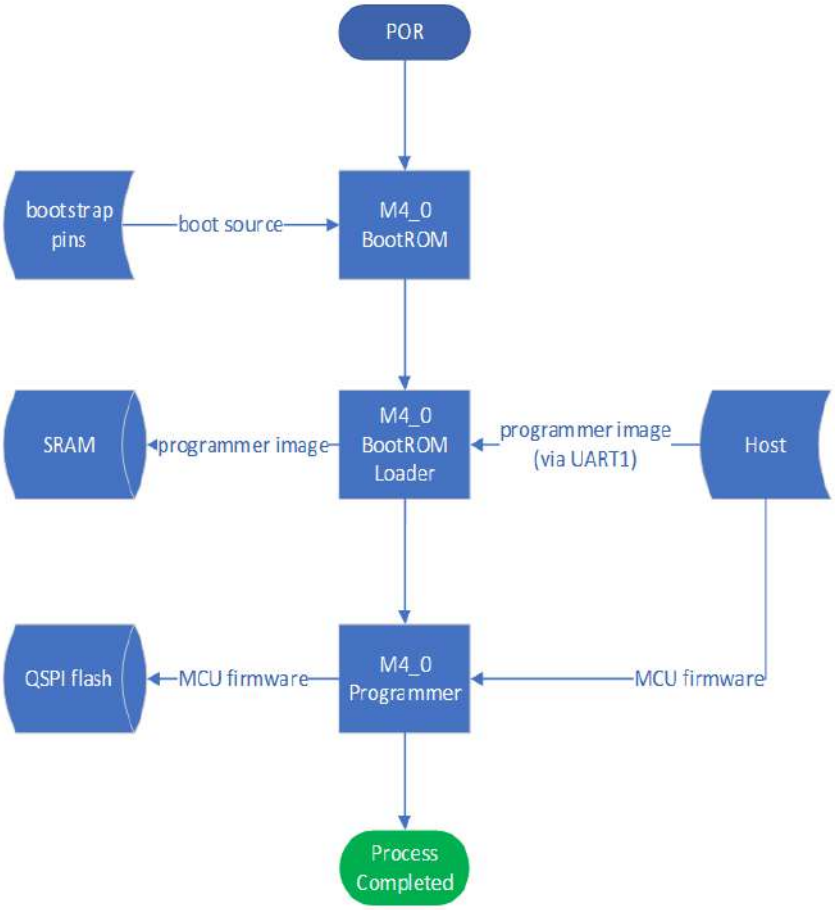


Figure 12. Boot from UART

Diagram showing Boot from UART flow, for initial fusing or device recovery using simple proprietary data transfer protocol over the UART1 interface.

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4.3. NN Core

The Hailo-10H NN Core enables efficient deployment of Deep NNs (DNNs) leveraging an architecture built around internal functional units called clusters.

Key features include:

- Up to 40 TOPs with 4-bit precision and up to TOPs with 4-bit precision.
- Six clusters that can be used to deploy multiple NNs.
  - Scalable compute, control and memory structure optimized for NN primitives.
  - Fully programmable architecture to allow instantiation of all common NN building blocks, based on available software support delivered by the Hailo Dataflow Compiler (this includes, but is not limited to, layers such as convolution, pooling, fully connected and activation).
  - Support for advanced NN architecture with native support for split, concatenation and add layers.
- Flexible I/O and interconnect. Up to 40 I/O channels to the NN core.
  Configurable interconnect between NN core inputs, outputs and pre/post units.
- Precision configurability, support 4/8/16-bit precision for weights and activations, configurable at layer granularity.
- Built-in support for weight and activation compression.
- Multi-network pipelines supporting fast switching between multiple models, enabling efficient execution of sequential or parallel network pipelines with minimal overhead.
- NN pre/post processing hardware accelerator used to offload the following functions from the host:
  - Up to 4 NMS engines
  - Bi linear interpolation engines
  - Reshape engines
  - Softmax/normalization engine

4.4. High Bandwidth Interfaces

4.4.1. Ethernet

Not currently supported, if you wish to use this feature , please contact your Hailo support.

The Hailo-10H provides an IEEE-802.3-2002-compliant Media Access Controller (MAC) for Ethernet LAN communications through an industry-standard Reduced Gigabit Media-Independent Interface (RGMII) or Reduced Media-Independent Interface (RMII). The Hailo-10H requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The MAC integrates a DMA, 1588 functionality, TSN/AVB and PCS for automotive applications.

Key features include:

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- 10/100/1000 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers from the memory (DRMA) to peripherals or from the peripheral to memory.
- Tagged MAC frame support (VLAN support)
- TCP/IP and UDP offload
- TCP segmentation and UDP fragmentation offload
- Receive segment coalescing offload
- MAC control sublayer (control frames)
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast addresses (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. Sizes of transmit and the receive FIFOs are 16KB and 4KB, respectively
- Hardware Precision Time Protocol (PTP) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Time Stamping Unit (TSU) supports a 102-bit timer
- Credit Based Shaping - TSN, 802.1Qav
- Enhanced Scheduled Traffic - TSN, 802.1Qbv
- Frame Replication and Elimination for Reliability - TSN, 802.1CB

4.4.2. PCI Express (PCIe)

Hailo-10H provides up to 4-lane PCI-SIG compliant PCIe® gen 3 PHY and controller, Endpoint or RC, enabling it to be integrated as a PCIe root complex. It also integrates a dedicated scatter-gather DMA for efficient memory mapped transactions.
PCIe requires a 100MHz clock oscillator on board for its reference clock.

Key features include:

- Up to 32 Gbps bi-directional throughput
  - X1/X2/X4 lanes
  - Shares one PHY with USB 3.x, therefore when USB is used, PCIe can use up X1/X2 lanes only.
  - Supports link rate of 2.5, 5.0, 8.0 GT/s per lane
- Lane reversal support
- L1 PM Sub-states with CLKREQ
- Latency Tolerance Reporting (LTR)
- Multiple endpoints support (through PCIe switch)
- Up to 2.5µs read latency from host memory in full BW

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- Supports also Device low power modes - D0, D3
- Up to 4K Byte maximum payload size
- Advanced Error Reporting (AER) support
- ECRC generation and check support
- MSI (up to 32 per device ID) support
- Internal DMA (32 channels) for host direct access to EP
- Retransmit and receive buffer of 2KB
- Up to 32 outstanding read requests
- Integrated safety mechanisms detecting transient and permanent faults in data and control paths.
- Full support for link power management including ASPM L0, ASPM L1, L1.1, L1.2 and L2
- Enhanced configuration access mechanism (ECAM) of 256MB support
- Up to 16 address translation tables (ATR) for indirect memory space access

4.4.3. Universal Serial Bus Interface

Hailo-10H contains an embedded USB 3.1 gen2 USB controller and PHY with a single port.

- USB 3.1 supports host\device modes
- Compliant with USB 3.1 and xHCI 1.1 specifications
- Supports link power modes for USB3 (U1/U2/U3)
- Supports SS, SS+ and protocols
- **In host mode:**
  - Supports up to 64 slots
  - Up to 128 periodic endpoints
  - 256 primary streams supported
  - MSI support
- **In device mode:**
  - Control transfers by EP#0
  - Up to 7 IN + 7 OUT programmable endpoints
  - Support also Device low power modes - D0, D3
  - Internal DMA for efficient memory access

4.4.4. Network on Chip (NoC)

The NoC is a homogeneous, scalable switch fabric network used as a central inter-connect fabric, running at approximately 1/4 of the DRAM data rate. It links the different sub-systems to DRAM controller for high-throughput DRAM access. The NoC includes Full End-to-End parity protection.

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4.5. Low Bandwidth Interfaces

4.5.1. Inter-Integrated Circuit (I2C)

Hailo-10H integrates up to four I2C interfaces.

Key features include:

- Each interface can be Master or Slave
- High and low-speed support
- Bandwidth
  - Fast mode, up to 400Kbps
  - High-speed mode, up to 3.4Mb/s

4.5.2. Quad Serial Peripheral Interface (QSPI)

Hailo-10H integrates a single QSPI controller to work with external Flash devices and SPI slaves.

Key support includes:

- Up to 4 external Chip Selects (CS)
- Up to 1Gb of external memory space
- SPI (x1), DSPI (x2) and QSPI (x4) modes
- DDR and SDR modes
- Boot from external Flash
- External device frequency of up to 50MHz
- External device minimal frequency of 6.25Mhz
- Supports SPI half duplex 4-wire interfaces to SPI slaves

4.5.3. Universal Asynchronous Receiver Transmitter (UART)

Hailo-10H integrates up to 4 UART interfaces with flow control signal support.

Key features include:

- 8-bit communication with parity and fixed at one stop bit
- Baud rate up to 2Mbaud

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4.6. MCU

Hailo-10H integrates two Cortex M4 cores with a memory subsystem.

4.6.1. Cortex M4 Cores

Each of the two Cortex M4 MCU cores is equipped with a Memory Protection Unit (MPU) and a Floating Point Accelerator Unit (FPU) engine.

The cores communicate with each other through mailbox and semaphore modules.

Key features include:

- MPU
- FPU
- Support for up to 200MHz frequency
- ARM core based on ARMv7 architecture
- Boot from external Flash, UART or PCIe by external boot strap pins.

4.6.2. Flash System

Hailo-10H can access external Flash devices either directly through the QSPI controller or through the Flash caching system. The Flash caching system can cache read only instruction memory up to 512B.

Key features include:

- Two-way 512B cache
- Up to 4MB of configurable memory cache.
- Configurable fetching
- Configurable ECC on the cached data

4.7. Application Processor

Hailo-10H integrates an application processor cluster, running the system OS and managing the dataflow. Composed of several main components:

- Quad-core ARM Cortex A53 processors
- 1MB L2 cache memory system
- ARM Generic Interrupts Controller (GIC-500)
- Generic System Timer
- Application Processor Watchdog

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4.7.1. Cortex A53

Consists of ARM A53 processor with 4 cores running at maximum frequency of 1.3 GHz, providing 12kDMIPS.

Key features include:

- ARM v8 architecture
  - ARM® CoreSight™-400 integrated
  - Support Aarch32 and Aarch64 execution states
  - EL0-EL3 exception levels
- L1 cache of 32KB per core for data and code
  - Includes cache protection
- Advanced SIMD and floating-point extension
- Cryptography extension
- Throttling support for low-power consumption
- System low power modes – D1/D2/D3

4.7.2. L2 Memory System

The L2 memory system includes the cache pipeline that maintains memory coherency between A53 cores.

Key features include:

- Size of cache is 1MB
  - Cache line of 64B
  - ECC protected (both tag and data)
  - 16-way set associative cache
- Snoop Control Unit (SCU) included
- Access Coherency Port (ACP) support
  - Mapped up to 4GB DDR memory space

4.7.3. Generic Interrupt Controller

Hailo-10H contains an ARM GIC-500, compliant with ARM GIC Architecture 3.0 specification.

Key features include:

- 128 physical interrupts signals for system management
- Software generated interrupts (SGI) for inter-core communication
- MSI support by interrupt translation tables for USB & PCIe

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4.7.4. Generic System Timer

Hailo-10H includes a generic timer for standard timer related functions of the application processor. Part of an always on domain it increments based on a fixed clock frequency and provides time of operation.

4.7.5. Application Processor Watchdog

Hailo-10H integrates a watchdog to monitor the Cortex A53 cores.

Key features include:

- 32-bit counter
- Configurable Interrupt threshold
- Configurable system reset threshold

4.8. DDR Controller

The Hailo-10H DDR controller supports the following:

- LPDDR4 and LPDDR4X memory types.
- Speeds up to 4266 MT/s
- 32-bit data bus (2 channels in lock-step mode)
- Inline ECC.
- One or two banks (up to 8GB memory)
- Half pipe (16-bit data bus)

4.8.1. DDR Direct Memory Access

The Hailo-10H DDR is used for:

- Fast data and movement from DDR to/from NN-core.
- Fast parameters fetch from DDR to NN-core.
- Fast data movement from DDR to DDR.
    - up to 48 channels in each direction.
    - QOS per channel (also supported in NoC and DDR controller subsystem)
    - Hardwire credit interface with the NN-core.
    - Supports optional scatter – gather scheme (linked list) on DDR side.
    - Supports optional contiguous data scheme for better DDR performance on DDR side.

4.9. System Peripherals

4.9.1. Temperature Sensor

The Hailo-10H temperature sensor is a high-precision low-power junction temperature sensor embedded in the chip. Typical temperature sensor applications may include clock speed optimization, power management and thermal management.

Key features include:

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- +/- 3.0°C accuracy
- 12-bit resolution (10-bit and 8-bit alternatives at lower accuracy), parallel or serial
- Signature response on demand
- Analog fault coverage

4.9.2. Voltage Monitor

Hailo-10H embeds two on-chip voltage monitors that are low-power self-contained blocks designed to monitor differential voltage levels within the core logic voltage domains.

Key features include:

- 16 monitoring points
- +/-1% accuracy
- Up to 14-bit resolution
- Digital interface
- Signature response on demand
- Analog fault coverage

4.9.3. DMA

The Hailo-10H integrates a general purpose DMA module, to easily move and copy data around the Hailo-10H AI Processor.

Key features include:

- Each DMA has 8 configurable channels.
- Transfer of Peripheral to Memory, Memory to Peripheral, Memory to Memory and Peripheral to Peripheral.
- Supports hardware handshake interfaces for I2C and UART modules

4.9.4. General-Purpose Input Output (GPIO)

Hailo-10H integrates up to 32 GPIOs. Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as a peripheral alternate function. Most of the GPIO pins are shared with digital alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence to avoid spurious writing to the I/O registers.

All timer counters can be frozen in debug mode.

4.9.5. Watchdog

The Hailo-10H integrates 2 watchdogs as a safety module to monitor the CPUs in the system.

Key features include:

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- 32-bit counter.
- Configurable Interrupt threshold
- Configurable system reset threshold

4.9.6. Mailbox

Hailo-10H integrates ARM PL-320 mailbox IP, used to transfer information between MCU cores and the application processor.

The mailbox includes 16 internal different mailboxes that can be used in parallel. Each internal mailbox corresponds to a dedicated request and acknowledge interrupt. It also encapsulates a corresponding message data register.

Mailbox can be used to perform both unicast and multicast messages.

4.9.7. Semaphore

Hailo-10H integrates eight semaphore units to control MCUs access to a common resource.

4.9.8. CRC Hardware Offload Engine

Hailo-10H includes an internal CRC generator and calculator to accelerate CRC calculation on data and control.

Key features include:

- Generate and check CRC
- CRC32/CRC16 polynomials
- CRC calculation on 32/16-bit data width

4.10. Security System

4.10.1. Features

Hailo-10H implements a wide range of security features for typical target applications.

The security subsystem includes:

- Secure boot
- Complete Life Cycle Management (LCM)
- User access to hardware-accelerated cryptographic algorithms
- Secure debug access according to the product life cycle
- Inner configurable firewall to block unexpected access to secure system regions

4.10.2. Lifecycle Management

Hailo-10H has lifecycle support for Hailo's production and integrator development processes, as well as for product deployment and Return Merchandise Authorization (RMA).

The debug interface lock depends on the lifecycle state.

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4.10.3. True Random Number Generator (TRNG)

Hailo-10H contains a TRNG that delivers 32-bit random numbers produced by an integrated analog circuit.

The TRNG is fully compliant with FIPS 140-2.

4.10.4. Cryptographic Accelerator

Hailo-10H contains a hardware authentication engine and an encryption/decryption engine that support the following algorithms:

- AES (128,192,256)
- SHA1/2
- RSA (2048,3072,4096)

The cryptographic accelerator can be used for secure boot, data-at-rest and data-in-transit.

4.10.5. Trusted Execution Environment (TEE)

The Hailo-10H TEE monitors and controls incoming and outgoing traffic inside the chip based on predetermined security rules set during software boot.

The Hailo-10H security system has a configurable hardware firewall. It protects access to peripherals inside the chip, internal SRAMs and external memory regions.

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