HAILO
Empowering Intelligence

Hailo-8™ Automotive Datasheet

Revision 1.8
August 2025

Part Numbers

Automotive: HNC18BA21BH

See Table 1 for ordering information.



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Documentation Control

History Table

Revision	Date	Description
0.1	30 August 2019	Created
0.2	15 October 2019	Package Changed to 17X17 HFCBGA400 Pinout Changes
0.3	28 February 2020	Added ordering information Added power modes Added automotive related content Pinout changes
0.4	18 March 2020	Renamed power rails: VDD_CORE_NN to VDDCORE and VDD_CORE to VDDTOP. Renamed VSS to GND. Removed VSS_IO, all VSS_IO occurrences were renamed to GND. Renamed FUSE_VQPS to FUSE_TOP_VQPS Removed the option to power VDDCORE with voltage lower than 0.8V Aligned DVP interface to 100 [MHz]. Updated preliminary ball-out to final. Updated preliminary ball-out to final, Clearer grouping of pin's according to functionality in Renamed FLASH_CLK to FLASH_SCLK Renamed I2C_CLK to I2C_SCL

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		Added PCIE power that was previously omitted Renamed PCIE power pins removed XCVR_AVDD PCIE power pins. Renamed CSI power pins Renamed PCIE power pins Removed XCVR_AVDD PCIE power pins. Renamed CSI power pins Aligned ESD ratings to JEDEC industry standard and reduced ECM class. added RMII as a physical connectivity option. removed “Analog test options” feature Revised ISP expected performance for Hailo-8™ in sections and input and output formats.
0.5	12 May 2020	General: Multiple pin name changes Removed ESD/tach-up section Added commercial and industrial part numbers. Added I2S pins Removed power up sequence – moved to board design guidelines document. Added AVDD_TS, AVDD_VS Added AVDD_TS, AVDD_VS Added USB power rails Added SDIO power rails Removed ambient temperature ratings from thermal ratings Added AVDD_TS, AVDD_VS Added ambient operating temperatures ranges

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		Added AVDD_TS, AVDD_VS Renamed power rails: VDDCORE to VDD_CORE and VDDTOP to VDD_TOP.
0.8	28 November 2021	Complete refactoring
0.9	23 March 22	Updated pin list
1.0	4 July 22	Analog power rails Maximum ratings of the Voltage and temperature sensors were changed Updated V_ESD (CDM)
1.1	December 2022	Corrected typos in Ball chart Section 2.2-U5 removed from GND Replaced V3 with A19 Section 2.2 U5 added to RESERVED
1.2	May 2023	Section 1.3 Addition of AEC-Q100 grade 2 qualification
1.3	August 2023	Section 4.3 updated Power-up sequence and timing requirements
1.4	October 2023	Updated system modes and usage scenarios
1.5	December 2023	Section 4.4.1 updated VDDIO to 300 mA Typo corrections on pin names PCIE_REFCLK and CSI_TX _CLK
1.6	August 2024	Addition of functional safety statement in the Features section. Updated Functional Assignment table
1.7	April 2025	Updated power rail voltage values Section 4.1.1

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1.8	August 2025	PCIe MaxPayload for Hailo-8 is 256 Byte

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Table of Contents

1. Overview 13
1.1. Introduction 13
1.2. General Description 13
1.3. Features 14
1.4. Applications 16
1.5. Block Diagram 17
1.6. Ordering Information 17
1.7. Mechanical Details 18
1.8. Glossary 20
2. Pinout Description 22
2.1. Pin Assignment 22
2.2. Functional Assignment 24
2.3. Pin Multiplex Specifications 31
2.3.1 GPIO Group [0-1] 32
2.3.2 GPIO Group [2-3] 33
2.3.3 GPIO Group [4-5] 34
2.3.4 GPIO Group [6-7] 35
2.3.5 GPIO Group [8-15] 36
2.3.6 GPIO Group [16-31] 38
3. Thermal Characteristics 41
4. Electrical Characteristics 42
4.1. Absolute Maximum Ratings 42
4.1.1 Power Rails 42
4.1.2 Thermal Ratings 44
4.2. Recommended Operating Conditions 44
4.3. Power-up Sequence 46
4.4. Power Consumption 48
4.4.1 Maximum Supply Current 48
4.4.2 Supply Current in Selected Test Cases 50

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4.4.3 Power Modes 50
4.5. Digital I/O DC Characteristics 52
4.6. PCIE Characteristics (DC And AC) 56
4.7. MIPI DPHY RX Characteristics 59
4.8. MIPI DPHY TX Characteristics 61
4.8.1 LP Characteristics 61
4.8.2 HS Characteristics 63
4.9. RGMII Characteristics 68
4.10. Reset Characteristics 69
5. Detailed Description 70
5.1. System Modes and Usage Scenarios 70
5.1.1 Hailo-8 as a Companion Device 70
5.2. Bootstraps 71
5.3. NN Core 72
5.4. High Bandwidth Interfaces 73
5.4.1 Ethernet 73
5.4.2 PCI Express (PCIe) 74
5.4.3 MIPI CSI 75
5.4.4 Camera Parallel LVCMOS Interface 76
5.5. Low Bandwidth Interfaces 77
5.5.1 Inter-Integrated Circuit (I2C) 77
5.5.2 Quad Serial Peripheral Interface (QSPI) 77
5.5.3 Universal Asynchronous Receiver Transmitter (UART) 77
5.6. MCU 78
5.6.1 Cortex M4 Cores 78
5.6.2 MCU Memory 78
5.7. Vision Subsystem 78
5.7.1 Image Signal Processing (ISP) 78
5.8. System Peripherals 80
5.8.1 Temperature Sensor 80

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5.8.2 Voltage Monitor 80
5.8.3 General-Purpose Input Output (GPIO) 80
5.8.4 Timer 81
5.8.5 Watchdog 81
5.8.6 Mailbox 81
5.8.7 Semaphore 82
5.8.8 CRC Hardware Offload Engine 82
5.9. Security System 82
5.9.1 Features 82
5.9.2 Lifecycle Management 82
5.9.3 True Random Number Generator (TRNG) 83
5.9.4 Cryptographic Accelerator 83
5.9.5 Trusted Execution Environment (TEE) 83
5.10. Safety 83
5.10.1 NN Core SMs 84
5.10.2 NN Core Safety Aggregator 85
5.10.3 SoC-Level Safety Aggregator 85

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List of Figures

Figure 1: Hailo-8 Block Diagram 17
Figure 2: Hailo-8 Package Views 18
Figure 3: Hailo-8 Ball Diagram 23
Figure 4: Power-up Sequence 47
Figure 5: RGMII Multiplexing & Timing Diagram – TX signals 69
Figure 6: RGMII Multiplexing & Timing Diagram – RX Signals 69
Figure 7: Hailo-8 as a Companion Device 70
Figure 8 - SoC-Level Safety Aggregator 86

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List of Tables

Table 1: Ordering Information 17
Table 2: Hailo-8 Package Dimensions 19
Table 3: Glossary 20
Table 4: Hailo-8 Functional Pin Assignment 24
Table 5: GPIO Group [0-1] Multiplex Options 32
Table 6: GPIO Group [2-3] Multiplex Options 33
Table 7: GPIO Group [4-5] Multiplex Options 34
Table 8: GPIO Group [6-7] Multiplex Options 35
Table 9: GPIO Group [8-15] Multiplex Options 36
Table 10: GPIO Group [16-31] Multiplex Options 38
Table 11: Thermal Resistance 41
Table 12: Absolute Maximum Power Rail Ratings 42
Table 13: Absolute Maximum Thermal Ratings 44
Table 14: Hailo-8 Operating Ranges 44
Table 15: Power-up Sequence Timing Requirements 47
Table 16: Maximum Supply Current 48
Table 17: Current Consumption from VDD_CORE, Normal Mode 50
Table 18: Low-Power Modes, Power Consumption 51
Table 19: Failsafe Digital Pin DC Characteristics 52
Table 20: Regular GPIOs DC Characteristics 54
Table 21: PCIe Gen1 Transmitter Characteristics 56
Table 22: PCIe Gen2 Transmitter Characteristics 56
Table 23: PCIe Gen3 Transmitter Characteristics 56
Table 24: PCIe Transmitter Data Rate Independent Characteristics 57
Table 25:PCIe Receiver Electrical Idle Detect Threshold 57
Table 26:PCIe Receiver Termination Characteristics 57
Table 27: MIPI RX DPHY Clock Lane LP Voltage and Timing Characteristics 59
Table 28: MIPI RX DPHY Data Lane LP Voltage and Timing Characteristics 59
Table 29: MIPI RX DPHY HS DC Differential Input Impedance 60
Table 30: MIPI TX DPHY Data Lane LP DC Characteristics 61
Table 31: MIPI TX DPHY Data Lane LP AC Characteristics 61
Table 32: MIPI TX DPHY Clock Lane LP DC Characteristics 62
Table 33: MIPI TX DPHY Clock Lane LP AC Characteristics 62
Table 34: MIPI TX DPHY Data Lane HS DC Characteristics 63
Table 35: MIPI TX DPHY Data Lane HS AC Characteristics 64

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Table 36: MIPI TX DPHY Clock Lane HS DC Characteristics 65
Table 37: MIPI TX DPHY Clock Lane HS AC Characteristics 66
Table 38: MIPI TX DPHY Data Lane HS AC Characteristics 66
Table 39: RGMII Timing Requirements 68

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1. Overview

1.1. Introduction

This datasheet provides a technical description of the automotive grade version of the Hailo-8 System on a Chip (SoC), an Artificial Intelligence (AI) processor. This document must be read in conjunction with the Hardware Integration Guide, and Safety Manual to ensure proper design.

1.2. General Description

The Hailo-8 SoC provides groundbreaking efficiency for neural network (NN) deployment based on unique design elements within the Hailo-8 NN Core, including:

- **Distributed memory fabric with purpose-built pipeline** elements that allow very low-power memory access during NN processing
- **Extremely efficient computational** elements that can be applied variably, as needed
- **Dataflow-oriented interconnect** that adapts to the structure of the NN and allows high resource utilization

The NN Core can be coupled with multiple industry-leading interfaces and subsystems to deliver high efficiency and high compute, leading-edge AI solutions.

Hailo-8 enables a broad range of applications by integrating an optimal mix of performance, low power and sophisticated video analytics processing.

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1.3. Features

- MCU
  - 2 ARM Cortex-M4 @ 200 MHz
  - 640 KB internal SRAM (ECC protected)
  - FPU, MPU
- Neural Processing Unit (NN Core)
  - Up to 26 [TOPS]
  - High-performance, Hailo NN multi-stream, multi-network core
  - Hardware offload engines for Deep Neural Networks (DNN) with pre and post processing:
    - Tensor manipulation (crop & resize, ROI pooling, reshape)
    - Non Maximum Suppression (NMS)
    - Bi-linear transformation
    - Softmax
- Chip2chip connection for high bandwidth and throughput NNs
- 4-lane PCI Express Gen3 endpoint with integrated PHY
- MIPI CSI 1.3, 2 RX and TX interfaces
  - Integrated 4-lane DPHY
  - 2.5 Gbps per lane
  - TX interfaces can be used as DSI TX
- Camera Parallel LVCMOS Interface: up to 24 bits wide @ 100MHz
- 1Gbps Ethernet controller, IEEE1588 compliant, 100/1000 Mbps
- 4 UARTs
- 4 I2C interfaces
- 4 timers
- 2 x multi-channel programmable DMA engines
- 32 configurable GPIOs with interrupt support
- Quad SPI Flash Interface
  - Up to 50MHz clock supported

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- Vision Subsystem
  - Image Signal Processor (ISP) for a single sensor
  - Input formats: RAW8, RAW10, RAW12, RAW14
  - Output formats: RGB888, YUV422
  - Maximum input resolution: 4096X4096 P
  - Throughput: 4k @ 40 FPS, 1080p @ 120 FPS
- Safety
  - NN Core built-in safety mechanisms (SMs)
  - Fully configurable SoC-level safety aggregator
  - Dedicated ERROR/FATAL output pads
- Security Features
  - Hardware crypto accelerators
  - Firewall
  - Secure ROM and boot
- Power, reset and clock management
- Voltage monitor
- Temperature monitor
- Package
  - 400-pin HFCBGA
  - 17mm x 17mm, 0.8mm pitch
- AEC-Q100 grade 2 qualified

Functional safety is available for selected, high-volume customers - please contact Hailo sales for more information. Functional safety includes all hardware and software mechanisms required to achieve the safety level (according to ISO 26262 standard or other).

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1.4. Applications

The Hailo-8 SoC enables a broad range of automotive applications, including:

- Advanced Driver Assistance Systems (ADAS): pedestrian detection, traffic sign recognition, lane detection and departure warning, automatic emergency braking, adaptive cruise control, forward collision warning and more. Hailo-8 can implement accurate and efficient perception for camera and other sensors
- Automated Driving: one or more Hailo-8 devices can implement perception, sensor fusion and other complex AI workloads to enable higher levels of autonomy for automated and semi-automated vehicles
- In-cabin monitoring: implement accurate driver and occupancy monitoring for safety and for enhancing in-vehicle experience

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1.5. Block Diagram

Figure 1 shows the subsystems and functional modules of the Hailo-8 SoC.

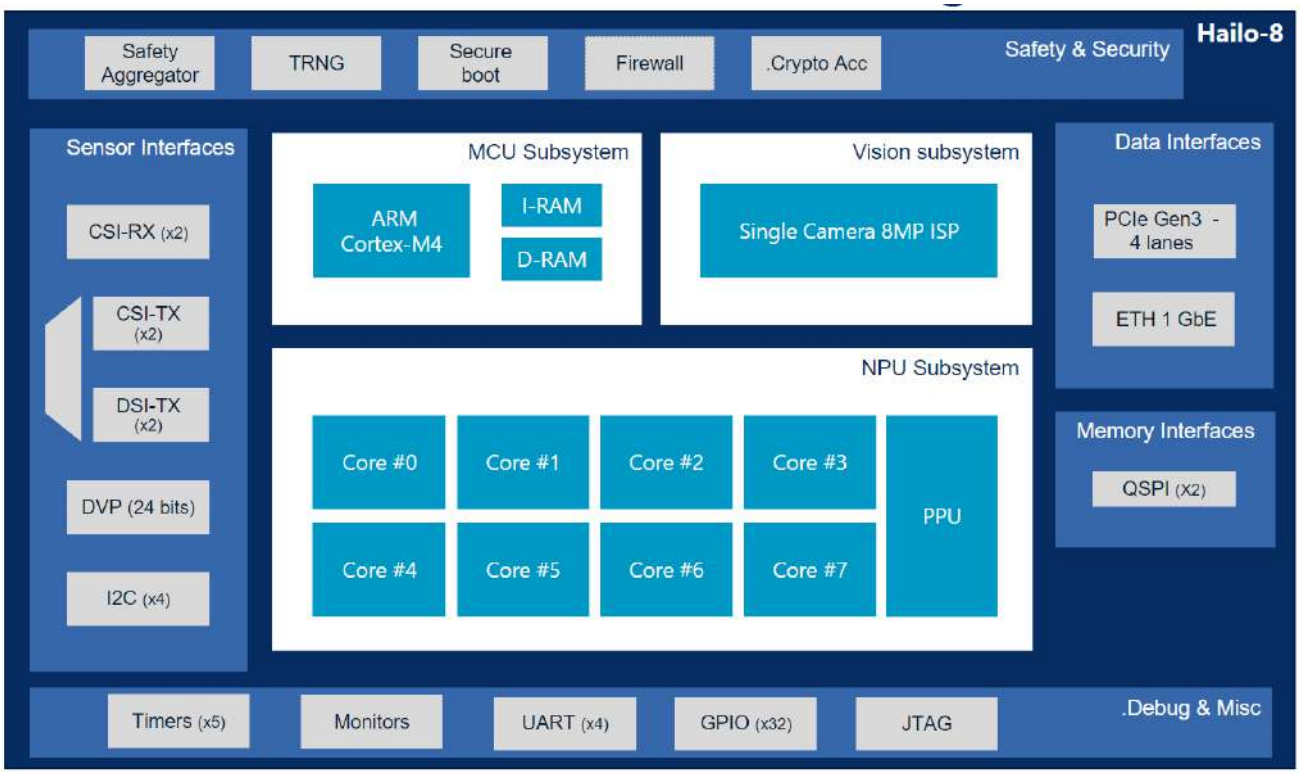


Figure 1: Hailo-8 Block Diagram

1.6. Ordering Information

Table 1: Ordering Information

Part Number	Device Grade	Temperature Range
HNC18BA21BH	Automotive	-40° to 105° C [1]

[1] Ambient temperature

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1.7. Mechanical Details

Figure 2 shows the top, bottom and side views of the 400-pin HFCBGA package.

Table 2 shows the package dimensions.

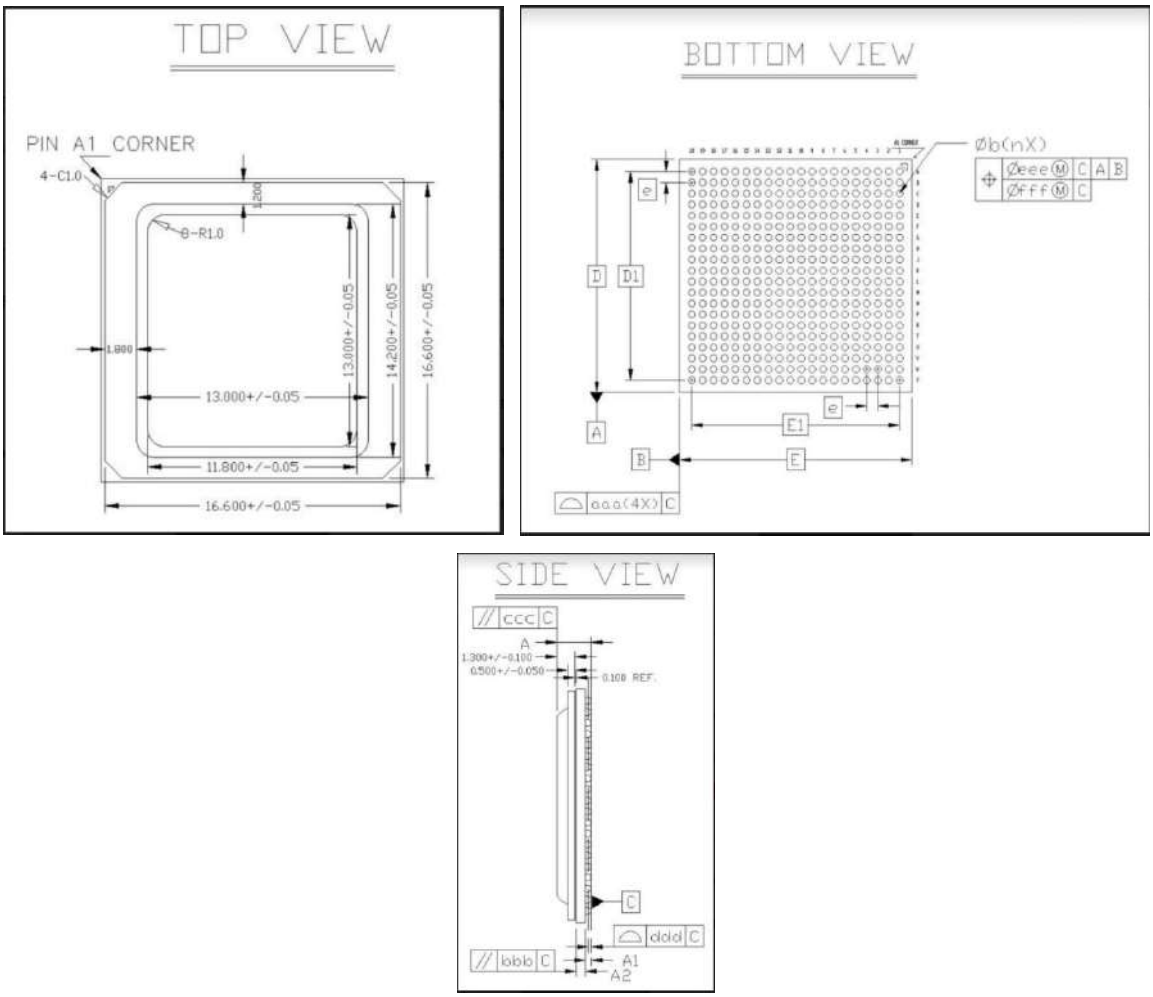


Figure 2: Hailo-8 Package Views

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Table 2: Hailo-8 Package Dimensions

Description	Symbol	Common Dimensions		
		Min	Nom	Max
Total thickness	A	2.326	2.476	2.626
Standoff	A1	0.300	-	0.500
Substrate thickness	A2	C676 Ref		
Thickness from substrate surface to die backside	A3	-		
Body size	E	17 BSC		
	D	17 BSC		
Ball diameter		C.500		
Ball width	b	0.400	-	0.600
Ball pitch	e	C.800 BSC		
Ball count	d	400		
Edge ball center to center	E1	15.200 BSC		
	D1	15.200 BSC		
Expose die size	E2	BSC		
	D2	BSC		
Package edge tolerance	aaa	C.200		
Substrate parallelism	bbb	C.250		
Top parallelism	ccc	C.350		
Coplanarity	ddd	C.150		
Ball offset (package)	eee	C.250		
Ball offset (ball)	fff	C.100		

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1.8. Glossary

Table 3 shows a list of the abbreviations used in this document.

Table 3: Glossary

Abbreviation	Description
BS	Boot strap
CMOS	Complementary Metal-Oxide
CS	Chip Select
CSI	Camera Serial Interface
DMA	Direct Memory Access
DNN	Deep Neural Network
DSI	Display Serial Interface
ECC	Error Correction Code
ETM	Electronic Trace Management
FPU	Floating Point Accelerator Unit
GPIO	General-Purpose Input Output
HS	High Speed
I/O	Input Output
I2C	Inter-Integrated Circuit
LP	Low Power
MCU	Microcontroller Unit
MIPI	Mobile Industry Processor Interface
MMU	Memory Management Unit
MPU	Memory Protection Unit
NMS	Non-Maximum Suppression
NN	Neural Network
PCIe	Peripheral Component Interconnect

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Abbreviation	Description
PHY	Physical Layer
PLL	Phase-Locked Loop
PVT	Process, Voltage, and Temperature
QSPI	Queued Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media-Independent Interface
ROI	Region of Interest
RoT	Root of Trust
RX	Receiver
SoC	System on a Chip
SM	Safety Mechanism
SRP	Session Request Protocol
TEE	Trusted Execution Environment
TOPS	Tera Operations Per Second
TX	Transmitter
UART	Universal Asynchronous Receiver

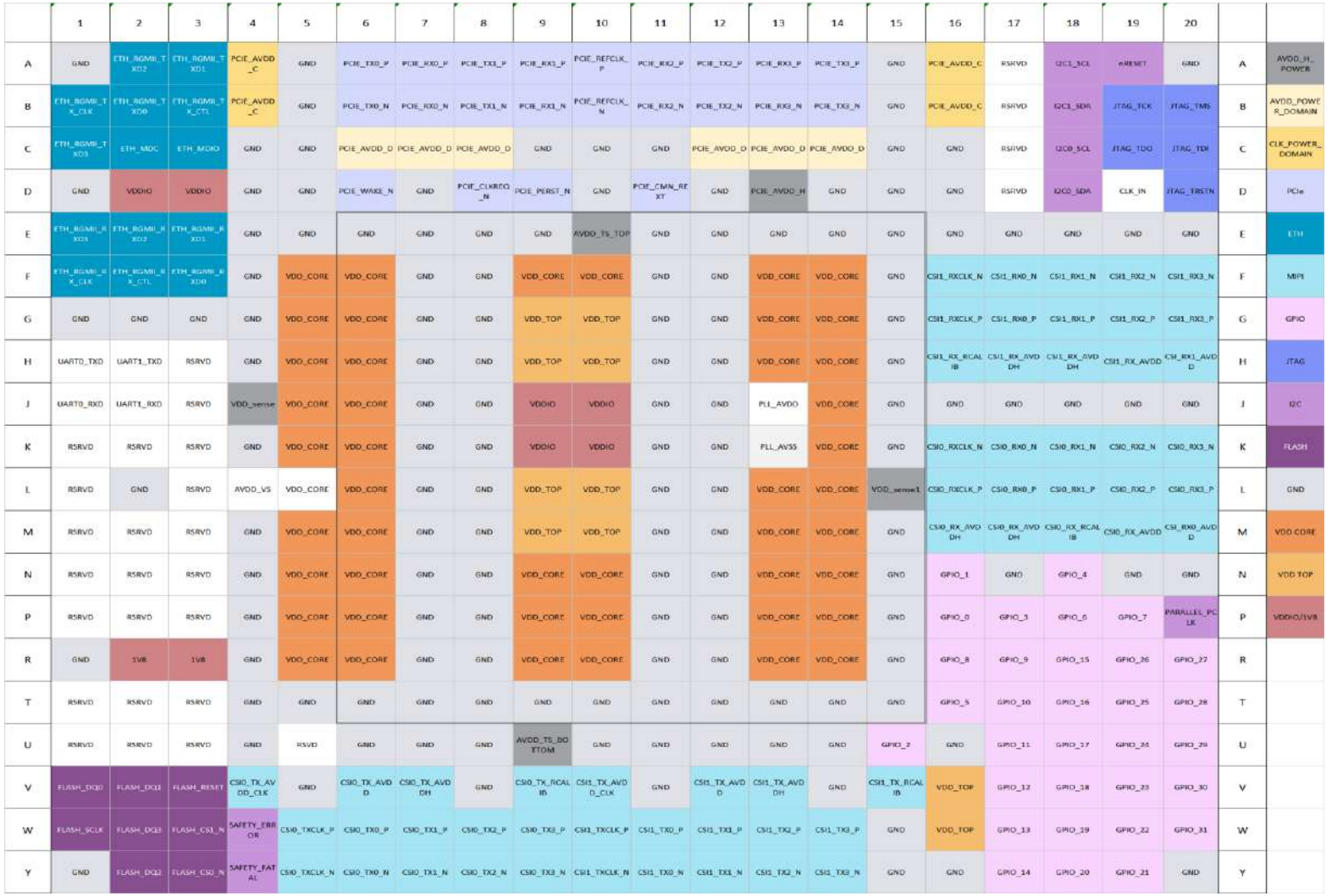
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2. Pinout Description

2.1. Pin Assignment

Figure 3 in the next page displays the schematic view of the Hailo-8 ball diagram.

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		
A	GND	ETH_RGMII_TXD2	ETH_RGMII_TXD1	PCIE_AVDD_C	GND	PCIE_TX0_P	PCIE_RX0_P	PCIE_TX1_P	PCIE_RX1_P	PCIE_REFCLK_P	PCIE_RX2_P	PCIE_TX2_P	PCIE_RX3_P	PCIE_TX3_P	GND	PCIE_AVDD_C	RSRVD	I2C1_SCL	nRESET	GND	A	AVDD_H_POWER
B	ETH_RGMII_TX_CLK	ETH_RGMII_TXD0	ETH_RGMII_TX_CTL	PCIE_AVDD_C	GND	PCIE_TX0_N	PCIE_RX0_N	PCIE_TX1_N	PCIE_RX1_N	PCIE_REFCLK_N	PCIE_RX2_N	PCIE_TX2_N	PCIE_RX3_N	PCIE_TX3_N	GND	PCIE_AVDD_C	RSRVD	I2C1_SDA	JTAG_TCK	JTAG_TMS	B	AVDD_POWER_DOMAIN
C	ETH_RGMII_TXD3	ETH_MDC	ETH_MDIO	GND	GND	PCIE_AVDD_D	PCIE_AVDD_D	PCIE_AVDD_D	GND	GND	GND	PCIE_AVDD_D	PCIE_AVDD_D	PCIE_AVDD_D	GND	GND	RSRVD	I2C0_SCL	JTAG_TDO	JTAG_TDI	C	CLK_POWER_DOMAIN
D	GND	VDDIO	VDDIO	GND	GND	PCIE_WAKE_N	GND	PCIE_CLKREQ_N	PCIE_PERST_N	GND	PCIE_CMN_REXT	GND	PCIE_AVDD_H	GND	GND	GND	RSRVD	I2C0_SDA	CLK_IN	JTAG_TRSTN	D	PCIe
E	ETH_RGMII_RXD3	ETH_RGMII_RXD2	ETH_RGMII_RXD1	GND	GND	GND	GND	GND	GND	AVDD_TS_TOP	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	E	ETH
F	ETH_RGMII_RX_CLK	ETH_RGMII_RX_CTL	ETH_RGMII_RXD0	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RXCLK_N	CSI1_RX0_N	CSI1_RX1_N	CSI1_RX2_N	CSI1_RX3_N	F	MIPI
G	GND	GND	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RXCLK_P	CSI1_RX0_P	CSI1_RX1_P	CSI1_RX2_P	CSI1_RX3_P	G	GPIO
H	UART0_TXD	UART1_TXD	RSRVD	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI1_RX_RCAL_IB	CSI1_RX_AVDDH	CSI1_RX_AVDDH	CSI1_RX_AVDD	CSI_RX1_AVDD	H	JTAG
J	UART0_RXD	UART1_RXD	RSRVD	VDD_sense	VDD_CORE	VDD_CORE	GND	GND	VDDIO	VDDIO	GND	GND	PLL_AVDD	VDD_CORE	GND	GND	GND	GND	GND	GND	J	I2C
K	RSRVD	RSRVD	RSRVD	GND	VDD_CORE	VDD_CORE	GND	GND	VDDIO	VDDIO	GND	GND	PLL_AVSS	VDD_CORE	GND	CSI0_RXCLK_N	CSI0_RX0_N	CSI0_RX1_N	CSI0_RX2_N	CSI0_RX3_N	K	FLASH
L	RSRVD	GND	RSRVD	AVDD_VS	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	VDD_sense1	CSI0_RXCLK_P	CSI0_RX0_P	CSI0_RX1_P	CSI0_RX2_P	CSI0_RX3_P	L	GND
M	RSRVD	RSRVD	RSRVD	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_TOP	VDD_TOP	GND	GND	VDD_CORE	VDD_CORE	GND	CSI0_RX_AVDDH	CSI0_RX_AVDDH	CSI0_RX_RCAL_IB	CSI0_RX_AVDD	CSI_RX0_AVDD	M	VDD_CORE
N	RSRVD	RSRVD	RSRVD	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_1	GND	GPIO_4	GND	GND	N	VDD_TOP
P	RSRVD	RSRVD	RSRVD	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_0	GPIO_5	GPIO_6	GPIO_7	PARALLEL_PCLK	P	VDDIO/1V8
R	GND	1V8	1V8	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	GND	GPIO_8	GPIO_9	GPIO_15	GPIO_26	GPIO_27	R	
T	RSRVD	RSRVD	RSRVD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GPIO_5	GPIO_10	GPIO_16	GPIO_25	GPIO_28	T	
U	RSRVD	RSRVD	RSRVD	GND	RSVD	GND	GND	GND	AVDD_TS_BOTTOM	GND	GND	GND	GND	GND	GPIO_2	GND	GPIO_11	GPIO_17	GPIO_24	GPIO_29	U	
V	FLASH_DQ0	FLASH_DQ1	FLASH_RESET	CSI0_TX_AVDD_CLK	GND	CSI0_TX_AVDD	CSI0_TX_AVDDH	GND	CSI0_TX_RCAL_IB	CSI1_TX_AVDD_CLK	GND	CSI1_TX_AVDD	CSI1_TX_AVDDH	GND	CSI1_TX_RCAL_IB	VDD_TOP	GPIO_12	GPIO_18	GPIO_23	GPIO_30	V	
W	FLASH_SCLK	FLASH_DQ3	FLASH_CS1_N	SAFETY_ERROR	CSI0_TXCLK_P	CSI0_TX0_P	CSI0_TX1_P	CSI0_TX2_P	CSI0_TX3_P	CSI1_TXCLK_P	CSI1_TX0_P	CSI1_TX1_P	CSI1_TX2_P	CSI1_TX3_P	GND	VDD_TOP	GPIO_13	GPIO_19	GPIO_22	GPIO_31	W	
Y	GND	FLASH_DQ2	FLASH_CS0_N	SAFETY_FATAL	CSI0_TXCLK_N	CSI0_TX0_N	CSI0_TX1_N	CSI0_TX2_N	CSI0_TX3_N	CSI1_TXCLK_N	CSI1_TX0_N	CSI1_TX1_N	CSI1_TX2_N	CSI1_TX3_N	GND	GND	GPIO_14	GPIO_20	GPIO_21	GND	Y	

Figure 3: Hailo-8 Ball Diagram

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2.2. Functional Assignment

The Hailo-8 functional pin assignment is described in Table 4.

Pin Types are categorized as follows:

- Power: SoC power rails
- I: input signals (Analog/Digital)
- O: output signals (Analog/Digital)
- OD: Open Drain IO

Table 4: Hailo-8 Functional Pin Assignment

Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger
Main Power and Sensing						
A1, A5, A15, A20, B5, B15, C4, C5, C9, C10, C11, C15, C16, D1, D4, D5, D7, D10, D12, D14, D15, D16, E4, E5, E6, E7, E8, E9, E11, E12, E13, E14, E15, E16, E17, E18, E19, E20, F4, F7, F8, F11, F12, F15, G1, G2, G3, G4, G7, G8, G11, G12, G15, H4, H7, H8, H11, H12, H15, J7, J8, J11, J12, J15, J16, J17, J18, J19, J20, K4, K7, K8, K11, K12, K15, L2, L7, L8, L11, L12, M4, M7, M8, M11, M12, M15, N4, N7, N8, N11, N12, N15, N17, N19, N20, P4, P7, P8, P11, P12, P15, R1, R4, R7, R8, R11, R12, R15, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, U4 ,U6, U7,	GND		Digital ground for device		Power	

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger
U8, U10, U11, U12, U13, U14, U16, V5, V8, V11, V14, W15, Y1, Y15, Y16, Y20						
F5, F6, F9, F10, F13, F14, G5, G6, G13, G14, H5, H6, H13, H14, J5, J6, J14, K5, K6, K14, L5, L6, L13, L14, M5, M6, M13, M14, N5, N6, N9, N10, N13, N14, P5, P6, P9, P10, P13, P14, R5, R6, R9, R10, R13, R14	VDDCORE		Digital supply for SoC NN core domain		Power	
G9, G10, H9, H10, L9, L10, M9, M10, V16, W16	VDDTOP		Digital supply for SoC top domain		Power	
D2, D3, J9, J10, K9, K10, R2, R3	VDDIO		Digital supply for IO pads		Power	
K13	PLL_VSSA		Analog ground for PLL		Power	
J13	PLL_VDDA		Analog supply for PLL		Power	
E10, U9	AVDD_TS		Analog supply for temperature sensor		Power	
L4	AVDD_VS		Analog supply for voltage sensor		Power	
J4	VDD_SENSE		Sense for VDDCORE		Sensing	
L15	VDD_SENSE1		Sense for VDDTOP		Sensing	
PCI Express (PCIe) Interface						
D6	PCIE_WAKE_N	I	PCIe wake signal to host		LVCMOS	

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger
D8	PCIE_CLKREQ_N	O	PCIe clock request to host	Drive 0	LVCMOS	
D9	PCIE_PERST_N	I	PCIe reset in	PD	LVCMOS	Yes
A6, A8, A12, A14	PCIE_TX[0:3]_P	I	PCIe positive signal of data transmit diff-pair		Analog	
B6, B8, B12, B14	PCIE_TX[0:3]_N	O	PCIe negative signal of data transmit diff-pair		Analog	
A7, A9, A11, A13	PCIE_RX[0:3]_P	I	PCIe positive signal of the data receive diff-pair		Analog	
B7, B9, B11, B13	PCIE_RX[0:3]_N	I	PCIe negative signal of data receive diff-pair		Analog	
B10	PCIE_REFCLK_N	I	PCIe ref clock in negative		Analog	
A10	PCIE_REFCLK _P	I	PCIe ref clock in positive		Analog	
D11	PCIE_CMN_REXT	I	PCIe calibration connection to external resistor		Analog	
A4, A16, B4, B16	PCIE_AVDD_C		Analog power for high-speed clock and digital functions		Power	
C6, C7, C8, C12, C13, C14	PCIE_AVDD_D		Clean analog power for high speed clock		Power	
D13	PCIE_AVDD_H		PCIe Analog I/O voltage		Power	
MIPI CSI TX Interface						
Y6, Y7, Y8, Y9	CSI0_TX[0:3]_N	O	Negative output of MIPI CSI TX interface[0] data lanes		Analog	
W6, W7, W8, W9	CSI0_TX[0:3]_P	O	Positive output of MIPI CSI TX interface data lane		Analog	
Y11, Y12, Y13, Y14	CSI1_TX[0:3]_N	O	Negative output of MIPI CSI TX interface[1] data lanes		Analog	
W11, W12, W13, W14	CSI1_TX[0:3]_P	O	Positive output of MIPI CSI TX interface[1] data lanes		Analog	
Y5, Y10	CSI[0:1]_TXCLK_N	O	Negative output of MIPI CSI TX interface clock		Analog	
W5, W10	CSI[0:1]_TXCLK_P	O	Positive output of MIPI CSI TX interface clock		Analog	
V9, V15	CSI[0:1]_TX_RCALIB	I/O	Pin connected to external resistor for calibrating on-SoC resistors for MIPI CSI TX interface		Analog	
V6, V12	CSI[0:1]_TX_AVDD		Analog power supply for MIPI CSI TX core		Power	
V7, V13	CSI[0:1]_TX_AVDDH		Analog power supply for MIPI CSI TX bias and PLL		Power	

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger
V4, V10	CSI[0:1]_TX_AVDD_CLK		Clean analog power supply for high-speed clock applications		Power	
MIPI CSI RX Interface						
K17, K18, K19, K20	CSI0_RX[0:3]_N	I	Negative input of MIPI CSI RX[0] interface data lane		Analog	
L17, L18, L19, L20	CSI0_RX[0:3]_P	I	Positive input of MIPI CSI RX[0] interface data lane		Analog	
F17, F18, F19, F20	CSI1_RX[0:3]_N	I	Negative input of MIPI CSI RX[1] interface data lane		Analog	
G17, G18, G19, G20	CSI1_RX[0:3]_P	I	Positive input of MIPI CSI RX[1] interface data lane		Analog	
K16, F16	CSI[0:1]_RXCLK_N	I	Negative input of MIPI CSI RX interface clock		Analog	
L16, G16	CSI[0:1]_ RXCLK_P	I	Positive input of MIPI CSI RX interface clock		Analog	
M18, H16	CSI[0:1]_RX_RCALIB	I/O	Pin connected to external resistor for calibrating on-SoC resistors for MIPI CSI RX interface		Analog	
M19, M20	CSI0_RX_AVDD		Analog power supply for MIPI CSI RX[0] core		Power	
H19, H20	CSI1_RX_AVDD		Analog power supply for MIPI CSI RX[1] core		Power	
M16, M17	CSI0_RX_AVDDH		Analog power supply for MIPI CSI RX[0] bias and PLL		Power	
H17, H18	CSI1_RX_AVDDH		Analog power supply for MIPI CSI RX[1] bias and PLL		Power	
Ethernet Interface						
B2, A3, A2, C1	ETH_RGMII_TXD [0:3]	O	Transmit data signal to PHY	Drive 0	LVCMOS	
B1	ETH_RGMII_TX_CLK	O	Transmit clock signal to PHY	Drive 0	LVCMOS	
B3	ETH_RGMII_TX_CTL	O	Transmit control signal to PHY	Drive 0	LVCMOS	
F3, E3, E2, E1	ETH_RGMII_RXD [0:3]	I	Receive data signal from PHY	PD	LVCMOS	Yes
F1	ETH_RGMII_RX_CLK	I	Receive clock signal from PHY	PD	LVCMOS	Yes
F2	ETH_RGMII_RX_CTL	I	Receive control signal from PHY	PD	LVCMOS	Yes
C2	ETH_MDC	O	Management interface clock	PD, Drive 0	LVCMOS	
C3	ETH_MDIO	I	Management interface Data input output	PU	LVCMOS	Yes

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger
Camera Parallel LVCMOS Interface						
P20	PARALLEL_PCLK	I	Parallel input clock	PD	LVCMOS	
Pin multiplexed with GPIOs	PARALLEL_VSYNC	I	Parallel VSYNC			
Pin multiplexed with GPIOs	PARALLEL_HSYNC	I	Parallel HSYNC			
Pin multiplexed with GPIOs	PARALLEL_DATA [0:23]	I	Parallel data in			
Flash Interface						
V3	FLASH_RESET	O	Flash reset out	PD, Drive 1	LVCMOS	
Y3, W3	FLASH_CS[0:1]_N	O	Flash chip select, active low	PU, Drive 1	LVCMOS	
Pin multiplexed with GPIOs	FLASH_CS[2:3]_N		Flash chip select, active low	PD		
V1, V2, Y2, W2	FLASH_DQ[0:3]	I	Flash data in/out		LVCMOS	
W1	FLASH_SCLK	O	Flash clock	Drive 0	LVCMOS	
Universal Asynchronous Receiver Transmitter (UART) Interface						
J1, J2	UART[0:1]_RXD	I	UART receive data	PD	LVCMOS	Yes
H1	UART[0]_TXD	I	UART transmit data	PD	LVCMOS	Yes
H2	UART[1]_TXD	HiZ	UART transmit data		LVCMOS	Yes
Inter-Integrated Circuit (I2C) Interface						
D18, B18	I2C[0:1]_SDA	I	I2C[0-1] serial data	PU	LVCMOS	
C18, A18	I2C[0:1]_SCL	I	I2C[0-1] clock	PU	LVCMOS	
Pin multiplexed with GPIOs	I2C[0:3]_CURRENT_	I/O	Fast mode I2C pin			
SRC_EN						
Pin multiplexed with GPIOs	I2C[2:3]_SDA	I/O	I2C[2-3] serial data			
Pin multiplexed with GPIOs	I2C[2:3]_SCL	O	I2C[2-3] clock			
Reset and Clock						
D19	CLK_IN	I	SoC main clock		LVCMOS	
A19	NRESET	I	Chip reset, active low	PD	LVCMOS	Yes

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger
JTAG						
C20	JTAG_TDI	I	JTAG data input	PU	LVCMOS	
C19	JTAG_TDO	O	JTAG data output	Drive 0, PD	LVCMOS	
B20	JTAG_TMS	I	JTAG mode select	PU	LVCMOS	
B19	JTAG_TCK	I	JTAG clock	PD	LVCMOS	
D20	JTAG_TRSTN	I	JTAG reset. Active low	PD	LVCMOS	Yes
GPIO						
P16, U15, P17, N18	GPIO[0, 2-4]	O	General configurable pins. Output during Bootup.	Drive 0	LVCMOS	
N16	GPIO[1]	O	General configurable pins. Output during Bootup.	Drive X	LVCMOS	
T16	GPIO[5]	O	General configurable pins. Output during Bootup.	Drive 1	LVCMOS	
P18, P19, R16, R17, V17, W17, Y17, R18, T18, U18, V18, W18, Y18, Y19, W19, V19	GPIO[6-9, 12-23]	I	General configurable pins	PD	LVCMOS	
T17, U17, U19, T19, R19, R20, T20, U20	GPIO[10-11, 24-29]	O	General configurable pins	Drive 0	LVCMOS	
V20, W20	GPIO[30-31]	O	General configurable pins	Drive 1	LVCMOS	
MCU GPIOS						
Pin multiplexed with GPIOs	MCU_GPIO[0-31]	I/O	GPIOs			
Timers						
Pin multiplexed with GPIOs	TIMER[0-3]_EXT_IN	I	External timer clock input			
Electronic Trace Management (ETM)						
Pin multiplexed with GPIOs	ETM_TRACE_CLOCK		ETM clock out			
Pin multiplexed with GPIOs	ETM_DATA[0-3]		ETM trace data out			
Miscellaneous						
H3, J3, U5	RSVD	I	Factory use only. Do not connect.			
M1, M2, K2	RSVD		Must be connected to GND on board			

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Pin Numbers	Pin Name	Default Direction	Description	Ball Reset State	Cell Type	Default Schmitt Trigger
M3	RSVD		Must be connected to ext. 1m ohm PD GND on board			
A17	BS_RSRVD	I	Must be connected to external 10K PD			
D17	BS_IO_SEL[0]	I	See section 5.2			
B17, C17, K1, K3, L1, L3	RSVD		Factory use only. Do not connect.			
P1, P2, P3, T1, T2, T3, U1, U2, U3, N1, N2, N3,	RSVD		Factory use only. Do not connect.			

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2.3. Pin Multiplex Specifications

This section describes the possible multiplex configurations available for Hailo-8 GPIOs. Each of the 32 GPIOs has up to 8 options.

Important: Each group of pins can only be set to the same option.

- Option1 – pads_pinmux_mode[3:0] = [0000]
- Option2 – pads_pinmux_mode[3:0] = [0010]
- Option3 – pads_pinmux_mode[3:0] = [0011]
- Option4 – pads_pinmux_mode[3:0] = [0100]
- Option5 – pads_pinmux_mode[3:0] = [0101]
- Option6 – pads_pinmux_mode[3:0] = [0110]
- Option7 – pads_pinmux_mode[3:0] = [0111]
- Option8 – pads_pinmux_mode[3:0] = [1000]
- Option9 – pads_pinmux_mode[3:0] = [1001]

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2.3.1 GPIO Group [0-1]

The multiplex options for GPIO[0] and GPIO[1] are listed in Table 5.

Table 5: GPIO Group [0-1] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO0	INITIAL_DEBUG_BUS [0]	GPIO[0]	I2C0_CURRENT_SRC_EN	FLASH_CS[2]	RSRVD	SAFETY_OUT0	RSRVD	UART2_TXD	I2C2_CURRENT_SRC_EN
GPIO1	INITIAL_DEBUG_BUS [1]	GPIO[1]	I2C1_CURRENT_SRC_EN	FLASH_CS[3]	RSRVD	SAFETY_OUT1	RSRVD	UART3_TXD	I2C3_CURRENT_SRC_EN

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2.3.2 GPIO Group [2-3]

The multiplex options for GPIO[2] and GPIO[3] are listed in Table 6.

Table 6: GPIO Group [2-3] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO2	INITIAL_DEBUG_BUS [2]	GPIO[2]	I2C0_CURRENT_SRC_EN	FLASH_CS [2]	RSRVD	SAFETY_OUT0	RSRVD	UART2_TXD	I2C2_CURRENT_SRC_EN
GPIO3	INITIAL_DEBUG_BUS [3]	GPIO[3]	I2C1_CURRENT_SRC_EN	FLASH_CS [3]	RSRVD	SAFETY_OUT1	RSRVD	UART3_TXD	I2C3_CURRENT_SRC_EN

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2.3.3 GPIO Group [4-5]

The multiplex options for GPIO[4] and GPIO[5] are listed in Table 7.

Table 7: GPIO Group [4-5] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8	Option9
GPIO4	INITIAL_DEBUG_BUS [4]	GPIO[4]	I2C0_CURRENT_SRC_EN	FLASH_CS[2]	RSRVD	SAFETY_OUT0	RSRVD	UART2_TXD	I2C2_CURRENT_SRC_EN
GPIO5	INITIAL_DEBUG_BUS [5]	GPIO[5]	I2C1_CURRENT_SRC_EN	FLASH_CS [3]	RSRVD	SAFETY_OUT1	RSRVD	UART3_TXD	I2C3_CURRENT_SRC_EN

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2.3.4 GPIO Group [6-7]

The multiplex options for GPIO[6] and GPIO[7] are listed in Table 8.

Table 8: GPIO Group [6-7] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7	Option8
GPIO6	PARALLEL_HSYNC	GPIO[6]	RSRVD	TIMER0_EXT_IN	TIMER2_EXT_IN	UART2_RXD	I2C2_SDA	I2C3_SDA
GPIO7	PARALLEL_VSYNC	GPIO[7]	RSRVD	TIMER1_EXT_IN	TIMER3_EXT_IN	UART3_RXD	I2C2_SCL	I2C3_SCL

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2.3.5 GPIO Group [8-15]

The multiplex options for GPIO[8] to GPIO[15] are listed in Table 9.

Table 9: GPIO Group [8-15] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO8	RSRVD	GPIO[8]	PARALLEL_DATA[0]	I2C2_SDA	TIMER0_EXT_IN	SAFETY_OUT0	FLASH_CS [2]
GPIO9	RSRVD	GPIO[9]	PARALLEL_DATA[1]	I2C2_SCL	TIMER1_EXT_IN	SAFETY_OUT1	FLASH_CS[3]
GPIO10	RSRVD	GPIO[10]	PARALLEL_DATA[2]	I2C3_SDA	RSRVD	I2C0_CURRENT_SRC_EN	UART2_RXD
GPIO11	RSRVD	GPIO[11]	PARALLEL_DATA[3]	I2C3_SCL	RSRVD	I2C1_CURRENT_SRC_EN	UART2_TXD
GPIO12	TIMER0_EXT_IN	GPIO[12]	PARALLEL_DATA[4]	SAFETY_OUT0	RSRVD	I2C2_CURRENT_SRC_EN	UART3_RXD

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GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO13	TIMER1_ EXT_IN	MCU GPIO[13]	PARALLEL_ DATA[5]	SAFETY_OU T1	RSRVD	I2C3_CURR ENT_ SRC_EN	UART3_TXD
GPIO14	TIMER2_ EXT_IN	MCU GPIO[14]	PARALLEL_ DATA[6]	PARALLEL_ HSYNC	RSRVD	PARALLEL_ HSYNC	PARALLEL_ HSYNC
GPIO15	TIMER3_ EXT_IN	MCU GPIO[15]	PARALLEL_ DATA[7]	PARALLEL_ VSYNC	RSRVD	PARALLEL_ VSYNC	PARALLEL_ VSYNC

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2.3.6 GPIO Group [16-31]

The multiplex options for GPIO[16] to GPIO[31] are listed in Table 10.

Table 10: GPIO Group [16-31] Multiplex Options

GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO16	UART2_RXD	GPIO[16]	PARALLEL_DATA[8]	PARALLEL_DATA[0]	Reserved	RSRVD	RSRVD
GPIO17	UART2_TXD	GPIO[17]	PARALLEL_DATA[9]	PARALLEL_DATA[1]	Reserved	RSRVD	RSRVD
GPIO18	UART3_RXD	GPIO[18]	PARALLEL_DATA[10]	PARALLEL_DATA[2]	Reserved	RSRVD	RSRVD
GPIO19	UART3_TXD	GPIO[19]	PARALLEL_DATA[11]	PARALLEL_DATA[3]	Reserved	RSRVD	RSRVD
GPIO20	I2C2_SDA	GPIO[21]	PARALLEL_DATA[12]	PARALLEL_DATA[4]	Reserved	RSRVD	UART2_RXD
GPIO21	I2C2_SCL	GPIO[21]	PARALLEL_DATA[13]	PARALLEL_DATA[5]	Reserved	RSRVD	UART2_TXD

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GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO22	I2C3_SDA	GPIO[22]	PARALLEL_DATA[14]	PARALLEL_DATA[6]	reserved	RSRVD	UART3_RXD
GPIO23	I2C3_SCL	GPIO[23]	PARALLEL_DATA[15]	PARALLEL_DATA[7]	Reserved	RSRVD	UART3_TXD
GPIO24	I2C0_CURRENT_SRC_EN	GPIO[24]	PARALLEL_DATA[16]	PARALLEL_DATA[8]	TIMER0_EXT_IN	RSRVD	RSRVD
GPIO25	I2C1_CURRENT_SRC_EN	GPIO[25]	PARALLEL_DATA[17]	PARALLEL_DATA[9]	TIMER1_EXT_IN	RSRVD	RSRVD
GPIO26	I2C2_CURRENT_SRC_EN	GPIO[26]	PARALLEL_DATA[18]	PARALLEL_DATA[10]	TIMER2_EXT_IN	RSRVD	I2C2_SDA
GPIO27	I2C3_CURRENT_SRC_EN	GPIO[27]	PARALLEL_DATA[19]	PARALLEL_DATA[11]	ETM_TRACE_CLK	RSRVD	I2C2_SCL
GPIO28	RSRVD	GPIO[28]	PARALLEL_DATA[20]	PARALLEL_DATA[12]	ETM_DATA[0]	RSRVD	I2C3_SDA

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GPIO	Option1	Option2	Option3	Option4	Option5	Option6	Option7
GPIO29	RSRVD	GPIO[29]	PARALLEL_DATA[21]	PARALLEL_DATA[13]	ETM_DATA[1]	RSRVD	I2C3_SCL
GPIO30	SAFETY_OUT0	GPIO[30]	PARALLEL_DATA[22]	PARALLEL_DATA[14]	ETM_DATA[2]	RSRVD	SAFETY_OUT0
GPIO31	SAFETY_OUT1	GPIO[31]	PARALLEL_DATA[23]	PARALLEL_DATA[15]	ETM_DATA[3]	RSRVD	SAFETY_OUT1

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3. Thermal Characteristics

Package thermal resistance at various junctions and under various airflow conditions is shown in Table 11. The board that achieved these results is defined by JEDEC (please refer to JEDEC standard JESD51-9, Test Board for Array Surface Mount Package Thermal Measurements) as follows:

- 8 PCB layers
- PCB dimensions [mm X mm] - 101.5 X 114.5
- PCB thickness [mm X mm] - 1.6 mm

Table 11: Thermal Resistance

Location	Airflow	Thermal Resistance (° C/W)
Junction to ambient $\boldsymbol{\theta_{JA_0}}$	No airflow	8.9
Junction to ambient $\boldsymbol{\theta_{JA_1}}$	1 m/s airflow	7.8
Junction to ambient $\boldsymbol{\theta_{JA_2}}$	2 m/s airflow	7.3
Junction to board $\boldsymbol{\theta_{JB}}$	No airflow	2.28
Junction to case $\boldsymbol{\theta_{JC}}$	No airflow	0.35

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4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 12 and Table 13 may cause permanent damage to the device and affect device reliability. These are stress ratings only and functional operation of the device at these conditions is not implied.

4.1.1 Power Rails

Table 12 provides the absolute maximum ratings of the power rails.

Table 12: Absolute Maximum Power Rail Ratings

Supply Name	Description	Min	Max	Unit
Digital Power Rails				
VDD_TOP	Top logic	-0.5	1.05	V
VDD_CORE	NN core	-0.5	1.05	V
VDDIO	IO banks	-0.5	2.5	V
MIPI DPHY Analog Power Rails				
CSI_RX_AVDD CSI_TX_AVDD	MIPI DPHY RX/TX core supply for analog and digital	-0.5	1.05	V
CSI_RX_AVDD_H CSI_TX_AVDD_H	High voltage power for the RX/TX analog, bias and PLL (PLL only for TX)	-0.5	2.5	V
CSI_TX_CLK	MIPI DPHY TX (only) clean core supply for analog high-speed clocking circuits	-0.5	1.05	V
PCIe PHY Analog Power Rails				
PCIE_AVDD_D	Analog power for non-high speed	-0.5	1.05	V

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Supply Name	Description	Min	Max	Unit
	clock and digital functions			
PCIE_AVDD_C	Clean analog power for high speed clock applications	-0.5	1.05	V
PCIE_AVDD_H	High voltage power for the bias and parts of the PLL	-0.5	2.5	V
Miscellaneous				
PLL_AVDD	PLL analog power rail	-0.5	1.05	V
FUSE_VQPS	Factory use only. Connect to GND.	-	-	V
AVDD_TS	Temperature sensor analog power rail	-0.5	2.5	V
AVDD_VS	Voltage sensor analog power rail	-0.5	2.5	V
Input voltage applied to digital IOs	Input Low Voltage	-0.5	2.5	V
V_ESD (HBM)	Electrostatic discharge voltage (Human Body Model)	2000		V
V_ESD (CDM)	Electrostatic discharge voltage (Charged Device Model)	250		V
Latch UP (LU)	class II of JESD78E immunity level	A[1]		-

1 Immunity level A: Pass the ±100mA and 1.5xVdd or MSV

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4.1.2 Thermal Ratings

Table 13 provides the storage and maximum junction temperature values.

Table 13: Absolute Maximum Thermal Ratings

Parameter	Description	Value	Unit
T_Storage	Storage temperature	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

4.2. Recommended Operating Conditions

Table 14 describes the recommended operating conditions for power rails, clocks and ambient temperature.

Table 14: Hailo-8 Operating Ranges

Supply Name	Description	Min	Nom	Max	Unit
Digital Domain Power Rails					
VDD_TOP	Top logic power rail	0.76	0.8	0.88	V
VDD_CORE	Neural Network Core Power rail	0.76	0.8	0.88	V
VDDIO	Digital Power Rail for IO banks	1.62	1.8	1.98	V
MIPI DPHY Analog Power Rails					
CSI_RX_AVDD CSI_TX_AVDD	MIPI RX/TX MIPI DPHY Core supply for analog and digital	0.76	0.8	0.88	V
CSI_RX_AVDD_H CSI_TX_AVDD_H	High voltage power for the RX/TX MIPI DPHY analog, bias and PLL (PLL only for TX)	1.62	1.8	1.98	V
CSI_TX_CLK	MIPI DPHY TX (only) clean core supply for analog high-speed clocking circuits	0.76	0.8	0.88	V

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Supply Name	Description	Min	Nom	Max	Unit
PCIe PHY Analog Power Rails					
PCIE_AVDD_D	Analog power for non-high speed clock and digital functions	0.76	0.8	0.88	V
PCIE_AVDD_C	Clean analog power for high speed clock applications	0.76	0.8	0.88	V
PCIE_AVDD_H	High voltage power for the bias and parts of the PLL	1.08	1.8	1.98	V
Other Power Rails					
PLL_AVDD	PLL analog power rail	0.76	0.8	0.88	V
FUSE_VQPS	Factory use only. Connect to GND.	-	-	-	V
AVDD_TS	Temperature sensor analog power rail	1.62	1.8	1.98	V
AVDD_VS	Voltage sensor analog power rail	1.62	1.8	1.98	V
External Clocks					
CLK_IN[1] Main Input clock signal (square wave)	Frequency	25±100PPM			MHz
	Duty Cycle	40	50	60	%
Ambient Operating Temperature					
T_A	Ambient Temperature	-40		105	°C

[1] CLK_IN clock pin must receive a square wave clock signal (oscillator output clock signal).

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4.3. Power-up Sequence

The power-up sequence should follow these guidelines:[1]

1. Initial state: NRESET pin is asserted (held low).
2. VDDIO rises to 1.8V. Slew rate should be less than 18V/ms.
3. VDD_CORE rises to 0.83V. VDD_CORE must hold VDD_CORE <VDDIO-0.3V. Slew rate of VDD_CORE should be less than 18V/ms.
4. PLL_VDDA should rise with VDD_CORE and be powered from VDD_CORE power regulator with filtering.
5. After the VDD_CORE reaches final level:
   a) Power-up CSI_RX/TX_AVDD and CSI_RX/TX_AVDDH. Each power ramp-up should be between 100us and 2ms. CSI_RX/TX_AVDDH and CSI_RX/TX_AVDD can power-up in any order.[2]
   b) Power-up PCIE_AVDD_D, PCIE_AVDD_C, PCIE_AVDD_H in any order. There are no timing limitations (minimum or maximum) when powering up multiple power supplies.
   c) PCIE_AVDD_D, PCIE_AVDD_C can be powered from VDD_CORE power regulator as long as noise target is met.[2]
   d) Power-up USB_VBUS, USB_AVDD_CORE, USB_AVDD_IO and USB_AVDD_IO_HV in any order.
      - There are no timing limitations (minimum or maximum) when powering up multiple power supplies.
      - Between the supplied and VBUS – there is no specific ramp up, and VBUS can be present in cases when there are both supplies and are no supplies provided to the USB 2.0[2] [2]
6. Enable reference clock after VDDIO reached final voltage level.

---

[1] T12 requirement derived from PCI Express Specification Rev 3.0, Section 2.6.2. AC Specifications:

Symbol	Parameter	Min	Max	Units	Notes
T_{PVPERL}	Power stable to PERST# inactive	100		ms	1

"De-asserted NRESET such having enough margin to the end point enter LTSSM Detect State within 20 ms of the end of Fundamental Reset (PERSTn) , and 100ms before system sending a Configuration Request to the device".

[2] On PCIe Only configuration – x_AVDD can be derived from with VDD_CORE, and x_AVDDH can be derived from VDDIO. Refer to 3.1.2.2 PCIe Only (Minimum Configuration).

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7. De-assert NRESET after clock is stable for 10 cycles. clock is stable when it meets the requirements for CLK_IN.
8. For PCIe application: De-assert NRESET before or up to 500us PCIe PERST is de-asserted. For non-PCIe application: Add 1K-2K PU on PERSTn

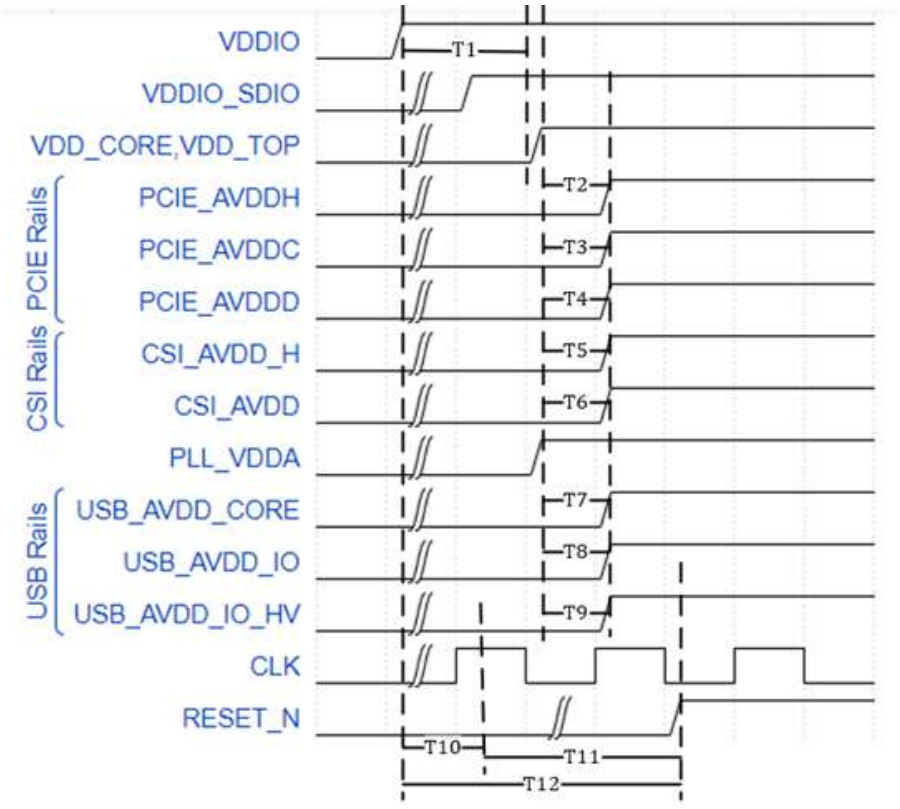


Figure 4: Power-up Sequence

Table 15: Power-up Sequence Timing Requirements

	Description	Min	Nom	Max	Unit
T1	VDDIO to VDD_CORE and VDD_TOP	1	-	-	us
T2	VDD_CORE to PCIE_AVDD_H	1	-	-	us
T3	VDD_CORE to PCIE_AVDD_C	1	-	-	us
T4	VDD_CORE to PCIE_AVDD_D	1	-	-	us
T5	VDD_CORE to CSI_AVDD_H	1	-	-	us
T6	VDD_CORE to CSI_AVDD	1	-	-	us
T7	VDD_CORE to USB_AVDD_CORE	1	-	-	us
T8	VDD_CORE to USB_AVDD_IO	1	-	-	us

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T9	VDD_CORE to USB_AVDD_IO_HV	1	-	-	us
T10	VDDIO to Stable Clock	1	-	-	ms
T11	Stable CLK to RESET_N de-assertion	100	-	-	us
T12	VDDIO to RESET_N de-assertion	-	-	70	ms

4.4. Power Consumption

4.4.1 Maximum Supply Current

The maximum current that can be drawn from each power rail is application-dependent. The measurements in Table 16 were made during device characterization and represent worst-case results across all PVT corners. The numbers are provided here only as general guidelines for power supply design.

Table 16: Maximum Supply Current

Supply Name	Max Current	Unit
VDD_CORE[1]	13	A
VDD_TOP	1.5	A
VDDIO[2]	0.3	A
CSI0_RX_AVDD	25	mA
CSI0_RX_AVDDH	30	mA
CSI1_RX_AVDD	25	mA
CSI1_RX_AVDDH	30	mA

1 The maximum current assumes heavy compute networks, for lowering the values, if needed, please evaluate the specific neural model and SoC integration for the specific network and add an adequate margin to cover all PVT corners and current spikes.

2 $VDDIO[V] \cdot \sum_{IO_i} \left(C_i[F] \cdot \frac{1}{2} \cdot f_{switching}[Hz] \right)$ Each IO_i drives a capacitance C_i[F] and is switched from 1 to 0 and vice versa at a frequency of 0.5f[Hz]. Add C_i[F]x0.5f[Hz] of all the IOs and multiply this sum by the VDDIO[V] voltage rail to obtain the VDDIO current consumption I_VDDIO[A].

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Supply Name	Max Current	Unit
CSI0_TX_AVDD	100	mA
CSI0_TX_AVDDH	14	mA
CSI0_TX_AVDD_CLK	10	mA
CSI1_TX_AVDD	100	mA
CSI1_TX_AVDDH	14	mA
CSI1_TX_AVDD_CLK	10	mA
PCIE_AVDD_D	280	mA
PCIE_AVDD_C	180	mA
PCIE_AVDD_H	21	uA
PLL_AVDD	1.2	mA
AVDD_TS	0.5	mA
AVDD_VS	0.3	mA

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4.4.2 Supply Current in Selected Test Cases

To demonstrate the current consumption dependency of the compute intensity, Table 17 presents current consumption of the VDD_CORE, measured while running the SoC in normal power mode with two widely adopted benchmarks.

Table 17: Current Consumption from VDD_CORE, Normal Mode

Test Condition	VDD_CORE Peak AC Current	VDD_CORE AVG Current	VDD_TOP AVG AC Current	VDD_TOP AVG Current	Unit
RESNET 50, 1328 FPS[1] TT, 25C, VDD_CORE=0.8V, VDD_TOP=0.8V	4.23	3.84	0.404	0.29	A
YOLO V3, 31 FPS[1] TT, 25C, VDD_CORE=0.8V, VDD_TOP=0.8V	6.24	2.69	0.46	0.33	A

4.4.3 Power Modes

When powered on, Hailo-8 can be operated in fully functional, normal mode or in any of three low-power modes: doze, sleep and hibernate.

Doze, sleep and hibernate modes are designed to help system integrators to optimally manage the exit latency vs. power tradeoff.

- **Doze** mode retains all memory and register-stored data to minimize reconfiguration time. The PLL remains powered-on to eliminate PLL lock time. Unused logic is clock-gated, and analog macros are held in the protocols' relevant low power states.
- **Sleep** mode minimizes power consumption more than Doze mode by powering off the PLL and the NN Core logic. This significantly reduces power requirements but requires additional wake-up time for PLL stabilization and register reconfiguration.
- **Hibernate** is the most aggressive low-power mode. It powers off NN

1 RESNET_v1_50 and YOLO V3 have been compiled and run with the Hailo SW Suite 2021-10. Compilation was performed using the Hailo Model Zoo; inference used HailoRT.

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Core memories in addition to NN Core logic and the PLL, requiring complete reconfiguration at wake-up.

See Table 18 for the power values of the three low-power modes.

Table 18: Low-Power Modes, Power Consumption

Mode	Power Consumption VDD_CORE + VDD_TOP [mW]
Doze	~70
Sleep	~30
Hibernate	~4.5

Note: VDDIO and all MIPI power rails can only be powered off when the SoC is powered off.

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4.5. Digital I/O DC Characteristics

There are two groups of I/O types:

1. Failsafe I/Os with strong PU/PD: Signals using this I/O type are: PCIE_PERST_N, PCIE_CLKREQ_N, PCIE_WAKE_N, GPIO0, GPIO1, CLK_IN and NRESET.
1. Regular I/Os: All other GPIOs use this I/O type.

Table 19 describes the DC characteristics of the failsafe digital pins as characterized across all PVT corners.

Table 19: Failsafe Digital Pin DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.35*VDD_IO	V
V_{IH}	Input High Voltage	0.65*VDD_IO		1.98	V
V_T	Threshold Point	0.91	1	1.13	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.97	1.09	1.2	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.75	0.86	0.97	V
V_{TPU}	Threshold point with Pull-Up Resistor Enabled	0.82	0.95	1.07	V
V_{TPD}	Threshold point with Pull-Down Resistor Enabled	0.91	1.01	1.14	V
V_{T+PU}	Schmitt Trigger Low to High Threshold Point with Pull-Up Resistor Enabled	0.87	1	1.13	V
V_{T-PU}	Schmitt Trigger High to Low Threshold Point	0.69	0.8	0.92	V

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Symbol	Parameter	Min	Typ	Max	Unit
	with Pull-Up Resistor Enabled				
V_{T+PD}	Schmitt Trigger Low to High Threshold Point with Pull-Down Resistor Enabled	0.98	1.09	1.22	V
V_{T-PD}	Schmitt Trigger High to Low Threshold Point with Pull-Down Resistor Enabled	0.75	0.86	0.98	V
I_L	Input Leakage Current @ Vi=1.8V or 0V			+/-10	uA
I_{OZ}	Tri-State Output Leakage Current @ Vi=1.8V or 0V			+/-10	uA
R_{PU}	Pull-Up Resistor	31	46	84	KΩ
R_{PD}	Pull-Down Resistor	31	44	71	KΩ
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
C	Output/Input capacitance	-	1.05	-	pF

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Table 20 describes the DC characteristics of the regular GPIOs pins, as characterized across all PVT corners.

Table 20: Regular GPIOs DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	-0.3		0.35*VDD_IO	V
V_{IH}	Input High Voltage	0.65*VDD_IO		1.98	V
V_{T}	Threshold Point	0.82	0.92	1	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.98	1.1	1.21	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.74	0.82	0.9	V
V_{TPU}	Threshold point with Pull-Up Resistor Enabled	0.82	0.91	1	V
V_{TPD}	Threshold point with Pull-Down Resistor Enabled	0.83	0.93	1.02	V
V_{T+PU}	Schmitt Trigger Low to High Threshold Point with Pull-Up Resistor Enabled	0.97	1.09	1.2	V
V_{T-PU}	Schmitt Trigger High to Low Threshold Point with Pull-Up Resistor Enabled	0.73	0.81	0.89	V
V_{T+PD}	Schmitt Trigger Low to High Threshold Point with Pull-Down Resistor Enabled	0.99	1.11	1.22	V

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Symbol	Parameter	Min	Typ	Max	Unit
V_{T-PD}	Schmitt Trigger High to Low Threshold Point with Pull-Down Resistor Enabled	0.75	0.83	0.91	V
I_L	Input Leakage Current @ Vi=1.8V or 0V			+/-10	uA
I_{OZ}	Tri-State Output Leakage Current @ Vi=1.8V or 0V			+/-10	uA
R_{PU}	Pull-Up Resistor	17	24	40	KΩ
R_{PD}	Pull-Down Resistor	17	23	36	KΩ
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
C	Output/Input capacitance for all other pads	-	0.88	-	pF

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4.6. PCIE Characteristics (DC And AC)

The following tables describe the PCIe characteristics as characterized across all PVT corners.

Table 21: PCIe Gen1 Transmitter Characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	876	1130	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	489.33	669.19	mV
LTX-SKEW	Lane-to-Lane Output Skew	-	0.438	ns

Table 22: PCIe Gen2 Transmitter Characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	810	1070	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	445	625	mV
LTX-SKEW	Lane-to-Lane Output Skew	-	0.235	ns

Table 23: PCIe Gen3 Transmitter Characteristics

Parameter	Description	Min	Max	Unit
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800	1010	mV
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	401	547	mV

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Parameter	Description	Min	Max	Unit
VTX-EIEOS-FS	Minimum voltage swing during EIEOS for full swing signaling	262	-	mVPP
VTX-EIEOS-RS	Minimum voltage swing during EIEOS for reduced swing signaling	256	-	mVPP
LTX-SKEW	Lane-to-Lane Output Skew	-	0.438	ns

Table 24: PCIe Transmitter Data Rate Independent Characteristics

Parameter	Description	Min	Max	Unit
VTX-AC-CM-PP	Tx AC peak-peak common mode voltage	-	134	mVPP
VTX-DC-CM	Tx DC peak-peak common mode voltage	0.396	0.404	V
VTX-CM-DC-LINE-DELTA	Absolute Delta of DC Common Mode Voltage between D+ and D-	2.1	7.2	mV
VTX-IDLE-DIFF-AC-p	Electrical Idle Differential Peak Output Voltage	8.09	19.98	mV
VTX-IDLE-DIFF-DC	DC Electrical Idle Differential Output Voltage	0.1	1.4	mV
ZTX-DIFF-DC	DC differential Tx impedance	69.2	75.3	Ω

Table 25:PCIe Receiver Electrical Idle Detect Threshold

Parameter	Description	Min	Max	Unit
VRX-IDLE-DET-DIFF-PP	Electrical Idle Detect threshold	92	154	mV

Table 26:PCIe Receiver Termination Characteristics

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Parameter	Description	Min	Max	Unit
ZRX-DC	Receiver DC single ended impedance	49.7	54.9	Ω
ZRX-HIGH-IMP-DC-POS (0-200 mV)	DC input CM input impedance for V≥0 during Reset or power-down	53k	-	Ω
ZRX-HIGH-IMP-DC-POS (> 200 mV)	DC input CM input impedance for V≥0 during Reset or power-down	144k	-	Ω
ZRX-HIGH-IMP-DC-NEG	DC input CM input impedance for V<0 during Reset or power-down	4.6k	-	Ω

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4.7. MIPI DPHY RX Characteristics

The following tables describe the MIPI RX DPHY characteristics as characterized across all PVT corners.

Table 27: MIPI RX DPHY Clock Lane LP Voltage and Timing Characteristics

Parameter	Description	Value	Unit
LP-RX Logic 1 Input Voltage (VIH)	Minimum voltage level where LP receiver consistently detects Logic 1	665	mV
LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	Maximum voltage level where non-ULP LP receiver consistently detects Logic 0	605	mV
LP-RX Input Hysteresis (VHYST)	Maximum Logic 1 hysteresis	25	mV
LP-RX Minimum Pulse Width Response (TMIN-RX)	Maximum Pulse width which LP receiver can detect without any error.	15	ns

Table 28: MIPI RX DPHY Data Lane LP Voltage and Timing Characteristics

Parameter	Description	Value	Unit
LP-RX Logic 1 Input Voltage (VIH)	Minimum voltage level where LP receiver consistently detects Logic 1	665	mV
LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	Maximum voltage level where non-ULP LP receiver consistently detects Logic 0	605	mV
LP-RX Input Hysteresis (VHYST)	Maximum Logic 1 hysteresis	25	mV
LP-RX Minimum Pulse Width c (TMIN-RX)	Maximum Pulse width which LP receiver can detect without any error	15	ns

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Table 29: MIPI RX DPHY HS DC Differential Input Impedance

Parameter	Description	Value	Unit
HS-RX DC Differential Input Impedance (ZID)	Data Lane: DC Differential Input Impedance (ZID)	100.1/122.9	Ohm
	Clock Lane: DC Differential Input Impedance (ZID)	102.9/117.1	Ohm

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4.8. MIPI DPHY TX Characteristics

The following tables describe the MIPI TX DPHY characteristics as characterized across all PVT corners.

4.8.1 LP Characteristics

Table 30: MIPI TX DPHY Data Lane LP DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Data Lane LP-TX Thevenin output high voltage level (VOH)	C_{LOAD} = 70 pF	0.969	1.153	1.217	V
Data Lane LP-TX Thevenin Output Low Level Voltage (VOL)	C_{LOAD} = 70 pF	-35	-0.87	49	mV

Table 31: MIPI TX DPHY Data Lane LP AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Data Lane LP-TX 15%-85% Rise Time (TRLP)	C_{LOAD} = 70 pF		18.136	21.02	ns
Data Lane LP-TX 15%-85% Fall Time (TFLP)	C_{LOAD} = 70 pF		17.66	22.04	ns
Data Lane LPTX Runtime XOR Clock Pulse Width (TLP-PULSE-TX)	C_{LOAD} = 70 pF	21.18	34.49		ns
Data Lane LPTX Runtime XOR Clock Pulse Width (TLP-PULSE-TX) (Initial)	C_{LOAD} = 70 pF	47.91	49.71		ns

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Parameter	Conditions	Min	Typ	Max	Unit
Data Lane LP-TX Period of Exclusive-OR Clock (TLP-PER-TX)	C_{LOAD} = 70 pF	92.83	97.06		ns
Data Lane Slew Rate Max	C_{LOAD} = 70 pF			115.9	mV/ns
Data Lane Slew Rate Min	C_{LOAD} = 70 pF	26.34	36.238		mV/ns
Data Lane Slew Rate Margin	C_{LOAD} = 70 pF	0.19	9.352		mV/ns

Table 32: MIPI TX DPHY Clock Lane LP DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane LP-TX Thevenin output High Voltage Level (VOH)	C_{LOAD} = 70 pF	1.036	1.185	1.23	V
Clock Lane LP-TX Thevenin Output Low Level Voltage (VOL)	C_{LOAD} = 70 pF	-36	-16.6	30	mV

Table 33: MIPI TX DPHY Clock Lane LP AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane LP-TX 15%-85% Rise Time (TRLP)	C_{LOAD} = 70 pF		18.27	23.23	ns
Clock Lane LP-TX 15%-85% Fall Time (TFLP)	C_{LOAD} = 70 pF		17.38	19.75	ns
Clock Lane Slew Rate Max	C_{LOAD} = 70 pF			113.98	mV/ns

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Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane Slew Rate Min	C_{LOAD} = 70 pF	34.57			mV/ns
Clock Lane Slew Rate Margin	C_{LOAD} = 70 pF	0.29			mV/ns

4.8.2 HS Characteristics

Table 34: MIPI TX DPHY Data Lane HS DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
HS Data TX Differential Voltage (VOD(0) Pulse)	Termination=80,100, 125 Ω Data rate = 2.5G,1G,1.5G,80Mbps	-263.4	-212	-176.5	mV
HS Data TX Differential Voltage (VOD(1) Pulse)		170.16	201.91	268.61	mV
Data Lane HS-TX Differential Voltage Mismatch (ΔVOD)		-13.93		2.73	mV
Data Lane HS-TX Single Ended Output High Voltage (VOHHS)			293.36	349.73	mV
Data Lane HS-TX Static Common-Mode Voltage (VCMTX)		158.9	172.7	248.27	mV
Data Lane HS-TX Static Common-Mode Voltage Mismatch (ΔVCMTX)				4.92	mV
Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz			9.02	23.15	mV_{PEAK}

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Parameter	Conditions	Min	Typ	Max	Unit
(ΔVCMTX(LF))					
Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz (ΔVCMTX(HF))			5.63	11.21	mV_{rms}

Table 35: MIPI TX DPHY Data Lane HS AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Data Lane HS-TX 20%-80% Rise time tR (bit rate <=1Gbps)	Termination=80,100,125 Ω Data rate = 2.5G,1G,1.5G,80Mbps	153.64	248.37	356.51	ps
Data Lane HS-TX 20%-80% Rise time tR (bit rate >1Gbps)		146.08	179.76	249.23	ps
Data Lane HS-TX 20%-80% Rise time tR (bit rate >1.5 Gbps)		105.55	124.24	145.73	ps
Data Lane HS-TX 80%-20% Fall time tR (bit rate< = 1Gbps)		182.27	248.4	356.13	ps
Data Lane HS-TX 80%-20% Fall time tR (bit rate >1Gbps)		145.55	179.34	240.22	ps
Data Lane HS-TX 80%-20% Fall time tR (bit rate > 1.5 Gbps)		107.14	125.83	148.87	ps

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Table 36: MIPI TX DPHY Clock Lane HS DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
HS Clock TX Differential Voltage(VOD(0) Pulse)	Termination=80,100,125 Ω Data rate = 2.5G,1G,1.5G,80Mbps				
HS Clock TX Differential Voltage(VOD(1) Pulse)		159.53	192.13	245.06	mV
Clock Lane HS-TX Differential Voltage Mismatch (Δ VOD)		-13.9		8.65	mV
Clock Lane HS-TX Single Ended Output High Voltage (VOHHS)			269.2	345.8	mV
Clock Lane HS-TX Static Common-Mode Voltage (VCMTX)		179.74	188.87	243.68	mV
Clock Lane HS-TX Static Common-Mode Voltage Mismatch (Δ VCMTX)			1.01	3.84	mV
Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz (Δ VCMTX(LF))			7.53	23.54	mV_{PEAK}

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Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz (Δ VCMTX(HF))			5.53	11.77	mV_{rms}

Table 37: MIPI TX DPHY Clock Lane HS AC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Clock Lane HS-TX 20%-80% Rise time tR (bit rate <=1Gbps)	Termination=80,100,125 Ω Data rate = 2.5G,1G,1.5G,80Mbps	186.29	232.91	296.69	ps
Clock Lane HS-TX 20%-80% Rise time tR (bit rate > 1Gbps)		144.94	171.32	243.25	ps
Clock Lane HS-TX 20%-80% Rise time tR (bit rate > 1.5 Gbps)		112.54	128.45	159.25	ps
Clock Lane HS-TX 80%-20% Fall time tR (bit rate< = 1Gbps)		188.54	231.1	292.18	ps
Clock Lane HS-TX 80%-20% Fall time tR (bit rate > 1Gbps)		143.11	168.71	241.65	ps
Clock Lane HS-TX 80%-20% Fall time tR (bit rate > 1.5 Gbps)		110.12	129.1	157.89	ps

Table 38: MIPI TX DPHY Data Lane HS AC Characteristics

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Parameter	Conditions	Min	Typ	Max	Unit
Data Lane HS-TX Single Ended Output impedance (ZOS)	Termination=80,100,125 Ω Data rate = 2.5G,1G,1.5G,80Mbps	40.61	51.75	55.92	Ω
Clock Lane HS-TX Single Ended Output impedance (ZOS)		40.67	49.25	53.58	Ω
Data Lane Single Ended Output Impedance Mismatch (delta ZOS)			1.06	9.94	%
Clock Lane Single Ended Output Impedance Mismatch (delta ZOS)			0.65	9.66	%
Data Lane LP-TX Output Impedance (ZOLP)		117.34	136.55		Ω
Clock Lane LP-TX Output Impedance (ZOLP)		116.31	135.05		Ω

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4.9. RGMII Characteristics

Meeting the timing requirements of the RGMII interface, as described here, is crucial for proper operation when interfacing RGMII compliant devices.

Table 39: RGMII Timing Requirements

Parameter	Description	Min	Typical	Max	Unit
T_cyc[1]	Clock cycle duration	7.2	8	8.8	ns
Duty_G[2]	Duty cycle for Gigabit mode	45	50	55	%
Duty_T[2]	Duty cycle for 100T mode	40	50	60	%
TskewT[3]	Data to clock output skew at transmitter	-500	0	500	ps
TskewR[3]	Data to clock input skew at receiver	1	1.8	2.6	ns
Tr / Tf	Rise/Fall time 20-80%	-	-	0.75	ns

See the Hardware Integration Guide for further design guidelines.

[1] For 100Mbps, Tcyc will scale to 40ns+-4ns.

[2] The duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain on condition that the minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest transitioning speed.

[3] This applies to all versions of RGMII prior to 2.0. This implies that PC board design will require clocks to be routed with an additional trace delay of greater than 1.5ns and less than 2.0ns, to be added to the associated clock signal. For 100Mbps, the maximum value is unspecified.

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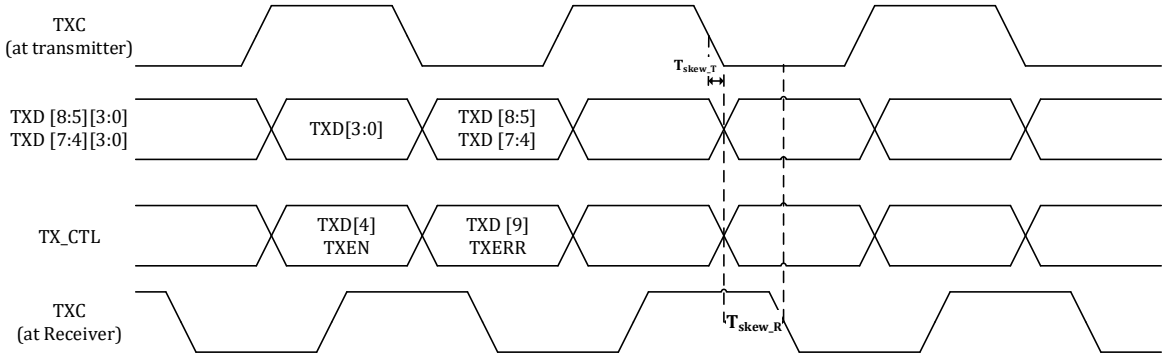


Figure 5: RGMII Multiplexing & Timing Diagram – TX signals

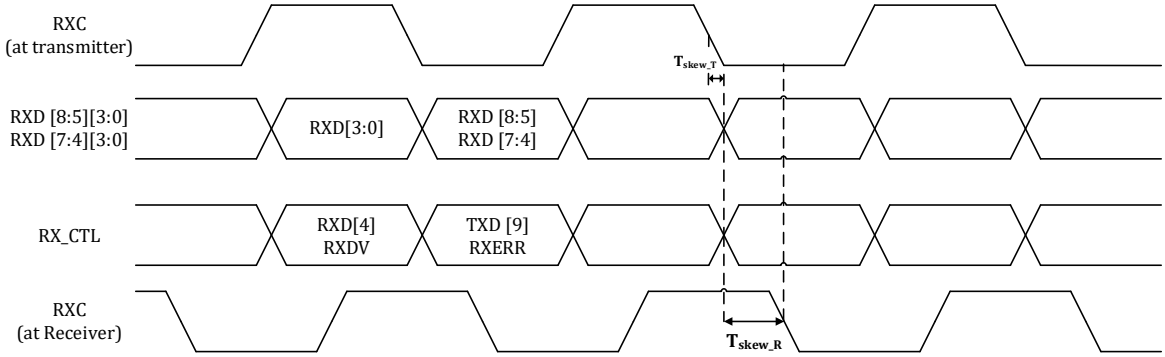


Figure 6: RGMII Multiplexing & Timing Diagram – RX Signals

4.10. Reset Characteristics

The NRESET pad should be driven by a Reset signal that meets the following requirements to provide Hailo-8 with a proper Reset pulse:

1. Rise and fall time (measured between 20% and 80% of VDDIO) < 5ns
2. NRESET assertion time (held low) >28us.

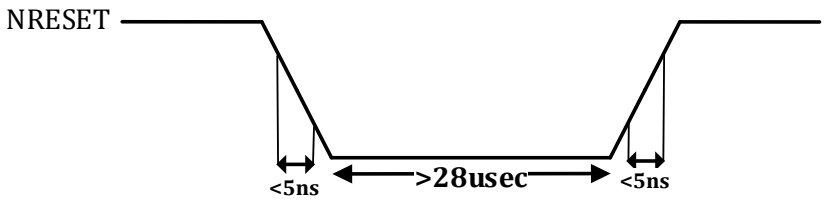


Figure 7: Reset Characteristics

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5. Detailed Description

This section describes various system modes and usage scenarios, and provides detailed information on various Hailo-8 subsystems.

See Hailo SW documentation for further elaboration.

https://hailo.ai/developer-zone/documentation/

5.1. System Modes and Usage Scenarios

5.1.1 Hailo-8 as a Companion Device

In companion mode, depicted in Figure 7, Hailo-8 is used to efficiently offload NN workload from the host application processor. It receives inference data and returns insights. Hailo-8 typically communicates with the application processor over PCIe.

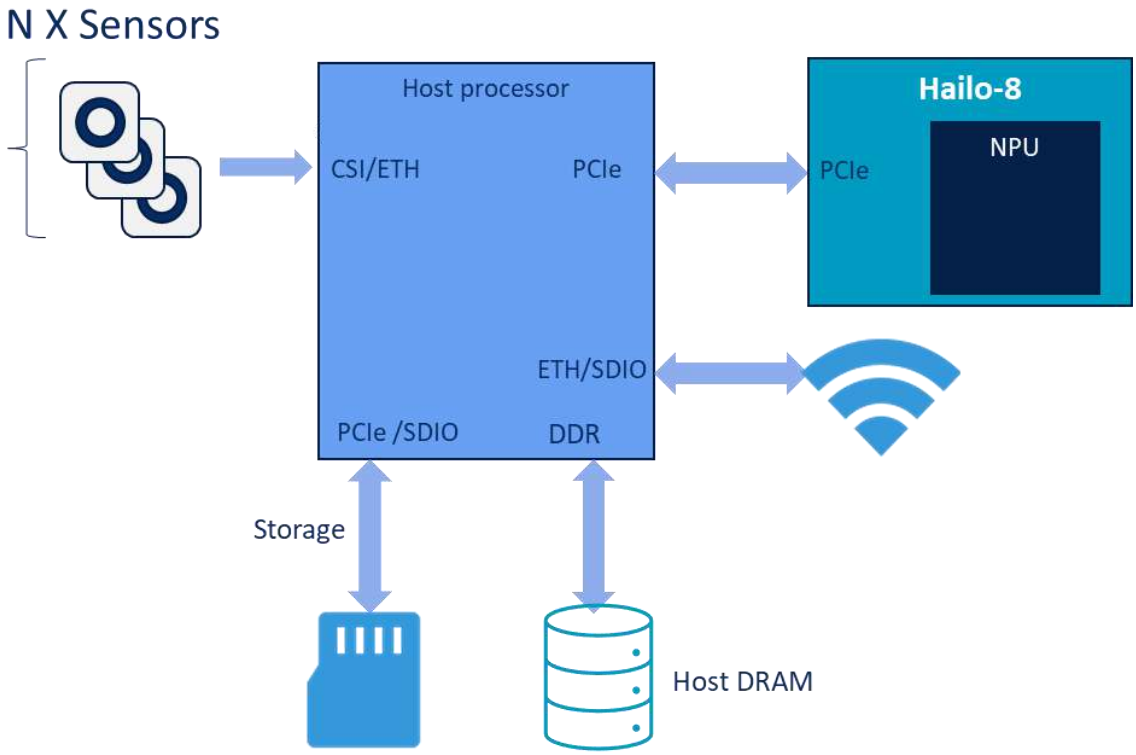


Figure 7: Hailo-8 as a Companion Device

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5.2. Bootstraps

Hailo-8 has one functional boot strap, called BS_IO_SEL[0], to enable the selection between two possible boot modes, PCIe when Boot Strap is pulled up, or Flash when Boot Strap is pulled down.

For PCIe boot, the SoC ROM handles the process with the host platform that runs the Hailo RT PCIe driver. Firmware is then fetched over the PCIe link to boot the device firmware.

For Flash boot, the SoC ROM fetches firmware from an on-board SPI flash device to complete the boot process.

The integrator can select the desired boot-flow according to dedicated system characteristics. See section 5.1 for further details.

See the Hardware Integration Guide for further implementation and bootstrap connectivity guidelines.

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5.3. NN Core

The Hailo-8 NN Core enables deployment of Deep NNs (DNNs) organized in eight internal functional units called clusters.

Key features include:

- Up to 26 TOPs, 8-bit precision
- Eight clusters that can be used to deploy multiple NNs
    - Compute, control and memory structure optimized for NN primitives
    - Fully programmable architecture to allow instantiation of all common NN building blocks, based on available software support delivered by the Hailo Dataflow Compiler (this includes, but is not limited to, layers such as convolution, pooling, fully connected and activation)
    - Support for advanced NN architecture with native support for split, concatenation and add layers
- Power modes
    - Normal (fully functional), doze, sleep and hibernate
    - Power shutdown can be executed at cluster level
- Up to 16 I/O channels to the NN core
- Configurable interconnect between NN core inputs, outputs and pre/post units
- 8/16-bit precision for both weights and activations, configurable at layer granularity
- 4-bit precision for weights, configurable at layer granularity
- NN pre/post processing hardware accelerator used to offload the following functions from host:
    - Up to eight pre/post processing configurable engines
    - NMS engine
        - Up to 128k proposals post score threshold
        - One comparison per cycle, two NMS engines may be aggregated to offer double throughput
        - Configurable intersection over union and score

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threshold with up to 16 threshold classes

- Bilinear interpolation engine
  - Streaming bilinear up to 8K resolution
  - Crop and Resize operations
- Reshape engine
  - Translates standardized formats to Hailo proprietary format and vice versa
  - Offloads advanced tensor reshape operations
- Softmax engine

5.4. High Bandwidth Interfaces

5.4.1 Ethernet

The Hailo-8 provides an IEEE-802.3-2002-compliant Media Access Controller (MAC) for Ethernet LAN communications through an industry-standard Reduced Gigabit Media-Independent Interface (RGMII) or Reduced Media-Independent Interface (RMII). The Hailo-8 requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The MAC integrates a DMA, 1588 functionality, TSN/AVB and PCS for automotive applications.

Key features include:

- 100, 1000 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers from the dedicated SRAM throughout the
- Tagged MAC frame support (VLAN support)
- TCP/IP and UDP offload
- MAC control sublayer (control frames)
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast addresses (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are each 2 Kbytes (4 Kbytes total)

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- Hardware Precision Time Protocol (PTP) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Time Stamping Unit (TSU) supports a 102-bit timer
- Credit Based Shaping - TSN, 802.1Qav
- Enhanced Scheduled Traffic - TSN, 802.1Qbv
- Frame Replication and Elimination for Reliability - TSN, 802.1CB

5.4.2 PCI Express (PCIe)

Hailo-8 provides a 4-lane PCI-SIG compliant PCIe gen 3 PHY and controller, enabling it to be integrated as a PCIe endpoint. It integrates a dedicated scatter-gather DMA for efficient memory mapped transactions.

Key features include:

- Up to 32 Gbps bi-directional throughput
  - X1/X2/X4 lanes
  - Supports link rate of 2.5, 5.0, 8.0 GT/s per lane
- Lane reversal support
- L1 PM Substates with CLKREQ
- Latency Tolerance Reporting (LTR)
- Single Physical Function
- Single Virtual Function
- Single Virtual Channel (VC)
- Up to $2.5\mu s$ read latency from host memory in full BW
- Support also Device low power modes - D0, D3
- Up to 256 Byte maximum payload size
- Advanced Error Reporting (AER) support
- ECRC generation and check support
- MSI (up to 32) and INT message support
- Internal DMA (32 channels)
- Dynamic Scatter-Gather DMA configuration, such as interrupt generation or start and end conditions for each specific SG page.

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- Core Context switch over PCIe – configuration and data
- FW boot from PCIe
- Control protocol
- Up to 16 dedicated RX and TX channels with low latency streaming FIFOs
- Supports out of order TLP arrival with integrated re-order buffer
- Retransmit buffer of 2KB
- Receive buffer of 2KB
- Up to 32 outstanding read requests
- Integrated safety mechanisms that detect transient and permanent faults in data and control paths
- Full support for link power management including ASPM L0, ASPM L1, L1.1 andL1.2

5.4.3 MIPI CSI

Hailo-8 integrates two MIPI CSI-RX v1.3 controllers and DPHY v1.2 with four lanes per DPHY, as well as two MIPI CSI-TX v1.3 controllers that are also equipped with DPHY v1.2 with four lanes per DPHY. This allows easy interfacing to sensors, displays and other SoCs. Each interface supports up to 10 Gbps throughput, for a total streaming throughput of 40 Gbps. The MIPI interfaces double as chip-to-chip interconnect, allowing a seamless expansion to the Hailo-8 NN core.

5.4.3.1 CSI-RX

The CSI-RX subsystem allows efficient streaming of pixel data to the Hailo-8 NN core. The CSI-RX is responsible for handling a CSI-2 protocol-based camera sensor or sensor data stream, and for unpacking the payload data and forwarding it to the pixel stream interfaces. The CSI-RX allows the selection of multiple independent input streams and supports the control of the destination for each stream (ISP or NN core).

Key features include:

- Operation modes:
    - High-Speed (HS): maximum up to 2.5Gbps per lane
    - Escape mode

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        - Remote triggers
        - LP-DT: up to 10Mbps
        - ULPS mode
- Supports up to four streams for each interface over distinct virtual channels and for different data types, which may be forwarded to different destinations in the NN Core or to the ISP.
- Supports the following data types:
    - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
    - RGB444, RGB555, RGB565, RGB666, RGB888
    - YUV8, YUV10

5.4.3.2 CSI-TX

The CSI-TX subsystem can process pixel data from a source and generate the CSI-2 data packets for short and long types. The CSI-TX also performs ECC/CRC generation and provides data support for frame and line counter packets.

The CSI-TX supports virtual channel and data type selection as well as all primary data types defined by MIPI CSI-2.

5.4.3.3 DSI-TX

The DSI-TX subsystem is intended to interface NN Core output data with a DSI compliant video mode display by embedding a DSI controller. This controller can be multiplexed by static configuration to feed data into the DPHY instead of using the CSI-TX controller.

5.4.4 Camera Parallel LVCMOS Interface

Hailo-8 integrates a camera parallel LVCMOS interface port of up to 24 bits wide at up to 100MHz, that connects to the video data bus from an image sensor.

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5.5. Low Bandwidth Interfaces

5.5.1 Inter-Integrated Circuit (I2C)

Hailo-8 integrates up to four I2C interfaces that may double as SCCB (Serial Camera Control Bus) interface to allow the device to be the Master that controls attached sensors.

Key features include:

- Each interface can be Master or Slave
- High and low-speed support
- Bandwidth
    - Fast mode, up to 400Kbps
    - High-speed mode, up to 3.4Mb/s

5.5.2 Quad Serial Peripheral Interface (QSPI)

Hailo-8 integrates a single QSPI to work with external Flash devices.

Key support includes:

- Up to two external Chip Selects (CS)
- Execute in Place (XIP) for external Flash device
- Up to 1Gb of external memory space
- SPI (x1), DSPI (x2) and QSPI (x4) modes
- DDR and SDR modes
- Boot from external Flash
- External device frequency of up to 50MHz

5.5.3 Universal Asynchronous Receiver Transmitter (UART)

Hailo-8 integrates up to four simple UART interfaces (no flow control signal support).

Key features include:

- 8-bit communication with parity and fixed at one stop bit

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- Baud rate up to 2Mbaud

5.6. MCU

Hailo-8 integrates two Cortex M4 cores with a memory subsystem.

5.6.1 Cortex M4 Cores

Each of the two Cortex M4 MCU cores is equipped with a Memory Protection Unit (MPU) and a Floating Point Accelerator Unit (FPU) engine.

The cores communicate with each other through mailbox and semaphore modules.

Key features include:

- MPU
- FPU
- Embedded Trace Microcell (ETM)
- Support for up to 200MHz frequency
- ARM core based on ARMv7 architecture
- Boot from external Flash or PCIe by external boot strap pins

5.6.2 MCU Memory

The MCU memory is accessible by both cores.

Key features include:

- Six data/code memory ports
- Total of 640KB SRAM memory for code and data with ECC
- 256KB ROM
- Up to 1Gb memory space for external Flash devices

5.7. Vision Subsystem

5.7.1 Image Signal Processing (ISP)

Hailo-8 integrates an ISP unit. It can be used to directly connect a CMOS sensor to the SoC.

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Key features include:

- Complete and fully configurable ISP pipeline
- Input formats:
  - RAW8, RAW10, RAW12, RAW14
- Output formats:
  - RGB888, YUV422
- 4k resolution: 40 fps videos
- 1080p resolution: 120 fps video
- Up to 4096h x 4096v resolution
- Optimized for low light environment applications
- Video statistics support Auto Focus, Auto White Balance, Auto Exposure
- On-the-fly defective pixel correction
- 10-bit Bayer channel gain supports up to x7.99
- Linear algebra for input pixel level adjustment
- Gb/Gr correction with maximum correction tolerance Gb/Gr rate of 12.5%
- 2D lens-shading correction (8x6)
  - Normal R/Gb/Gr/B channel shading correction
  - Color stain correction
- High resolution RGB interpolation: ES/Hue-Med/Average/Non-Direction based hybrid type algorithm
- Color correction matrix (3x3)
- Bayer gamma correction (19 points)
- High-performance noise reduction for low light environment: Bayer/RGB/YC domain
- High-resolution sharpness control: Multi-sharp filter and individual sharp gain control
- Color enhancement: hue, saturation, Delta-L control (RGBCMY)
- Auto Exposure: supports 16x16 luminance weight window and pixel weighting

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- Auto white balance: RGB-based feed-forward method Tone mapping: multi-band scheme using liner transformation as multi-slope
- Auto Focus (AF): 2-type 6-region AF value return

5.8. System Peripherals

5.8.1 Temperature Sensor

The Hailo-8 temperature sensor is a high-precision low-power junction temperature sensor embedded in the chip. Typical temperature sensor applications may include clock speed optimization, power management and thermal management.

Key features include:

- +/- 3.0°C accuracy
- 12-bit resolution (10-bit and 8-bit alternatives at lower accuracy), parallel or serial
- Signature response on demand
- Analog fault coverage

5.8.2 Voltage Monitor

Hailo-8 embeds two on-chip voltage monitors that are low-power self-contained blocks designed to monitor differential voltage levels within the core logic voltage domains.

Key features include:

- 16 monitoring points
- +/-1% accuracy
- Up to 14-bit resolution
- Digital interface
- Signature response on demand
- Analog fault coverage

5.8.3 General-Purpose Input Output (GPIO)

Hailo-8 integrates up to 32 GPIOs. Each of the GPIO pins can be

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configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as a peripheral alternate function. Most of the GPIO pins are shared with digital alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O alternate function configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/O registers.

5.8.4 Timer

Hailo-8 integrates four timers that can be programmed through the GPIO interfaces.

Key features include:

- 32-bit counter
- Clock from external clock input or internal clock
- Interrupt output to MCU system

All timer counters can be frozen in debug mode.

5.8.5 Watchdog

Hailo-8 integrates two watchdogs to monitor the MCUs in the system.

Key features include:

- 32-bit counter
- Configurable Interrupt threshold
- Configurable system reset threshold

5.8.6 Mailbox

Hailo-8 integrates eight mailboxes to transfer information between MCU cores.

Each mailbox has one data register to pass pointers to data between MCUs. After one MCU successfully writes data to the mailbox, the other MCU receives an interrupt.

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5.8.7 Semaphore

Hailo-8 integrates eight semaphore units to control access to a common resource.

5.8.8 CRC Hardware Offload Engine

Hailo-8 includes an internal CRC generator and calculator to accelerate CRC calculation on data and control.

Key features include:

- Generate and check CRC
- CRC32/CRC16 polynomials
- CRC calculation on 32/16-bit data width

5.9. Security System

5.9.1 Features

Hailo-8 implements a wide range of security features for typical target applications.

The security subsystem includes:

- Secure boot
- Complete Life Cycle Management (LCM)
- User-provided non-volatile hash (enabling RoT behavior)
- User access to hardware-accelerated cryptographic algorithms
- Secure debug access according to the product life cycle
- Inner configurable firewall to block unexpected access to secure system regions

5.9.2 Lifecycle Management

Hailo-8 has lifecycle support for Hailo's production and integrator development processes, as well as for product deployment and Return Merchandise Authorization (RMA).

The debug interface lock depends on the lifecycle state.

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5.9.3 True Random Number Generator (TRNG)

Hailo-8 contains a TRNG that delivers 32-bit random numbers produced by an integrated analog circuit.

The TRNG is fully compliant with FIPS 140-2.

5.9.4 Cryptographic Accelerator

Hailo-8 contains a hardware authentication engine and an encryption/decryption engine that support the following algorithms:

- AES (128,192,256)
- SHA1/2
- RSA (2048,3072,4096)

The cryptographic accelerator can be used for secure boot, data-at-rest and data-in-transit.

5.9.5 Trusted Execution Environment (TEE)

The Hailo-8 TEE monitors and controls incoming and outgoing traffic inside the chip based on predetermined security rules set during software boot.

The Hailo-8 security system has a configurable hardware firewall. It protects access to peripherals inside the chip, internal SRAMs and external memory regions.

5.10. Safety

Hailo-8 was designed according to the ISO-26262 standard to meet ASIL-B requirements. It features a wide range of built-in safety mechanisms (SMs) to detect and/or correct permanent and transient faults in all device domains and modules.

The key SoC-level SMs include:

- Parity protection for SoC interconnect
- Transaction timeout for main buses
- ECC memory protection

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- CRC hardware engine
- Watchdog timers
- Parity protection of safety-critical registers
- Fast data interface SMs
- Proprietary NN-aware SMs

For additional Hailo-8 safety documentation, please submit request at this link: https://hailo.ai/contact-customer-support/.

5.10.1 NN Core SMs

The NN Core embeds multiple proprietary SMs that reside in all NN Core hierarchies (sub-clusters, clusters, NN Core top, interconnect, memories etc.).

The NN Core SMs are:

- Top-Level SMs
    - Data Stream protection
      Protects NN Core top interconnect and NN Core top-level input and output buffering from both permanent and transient faults.
    - Redundant Allocation
      full redundancy for the NN-Core computational path, to increase diagnostic coverage of both permanent and transient faults.
- Cluster-Level SMs
    - Inter Layer protection
      Protects the interconnection between two layers, as well as NN Core top-level inter-layer buffering, from both permanent and transient faults.
    - Redundant Data Calculation
      Protects cluster and sub-cluster computational logic and interconnect from permanent faults.
    - Instruction Memory Address protection
      Prevents faulty addressing of the Layer Controller Unit (LCU) memory, which drives the layer
    - LCU Memory ECC

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- Sub-Cluster-Level SMs
    - Weights CRC Protection
      Protects weights against permanent and transient faults that may occur in memory.
    - Contexts CRC protection
      Protects intermediate results from permanent and transient faults that may occur in memory.

5.10.2 NN Core Safety Aggregator

The NN Core safety aggregator is multi-level, configurable hardware that aggregates all NN Core proprietary SM indications. Each SM for each component can be selectively masked and assigned as fatal or non-fatal. The final output of these modules is routed to the INT signals Nn_Core_Fatal and NN_Core_Non_Fatal, which are then routed to the SoC-level safety aggregator.

5.10.3 SoC-Level Safety Aggregator

The SoC-level safety aggregator aggregates all safety indications, both fatal and non-fatal, from the NN Core safety aggregator and other blocks. Block-level safety indications are usually aggregated to one/two INT signals which are routed to the SoC-level Safety Aggregator. For most blocks, the Safety indications are separated to Fatal/Non-Fatal in block's internals. Nevertheless, for maximal flexibility, each such indication can be unmasked, to be accounted for Fatal/Non-fatal/both SoC-level INT.

These indications may be routed directly to dedicated pads, multiplexed pads or to the MCU Core that can drive the safety pads based on pre-programmed decision logic.

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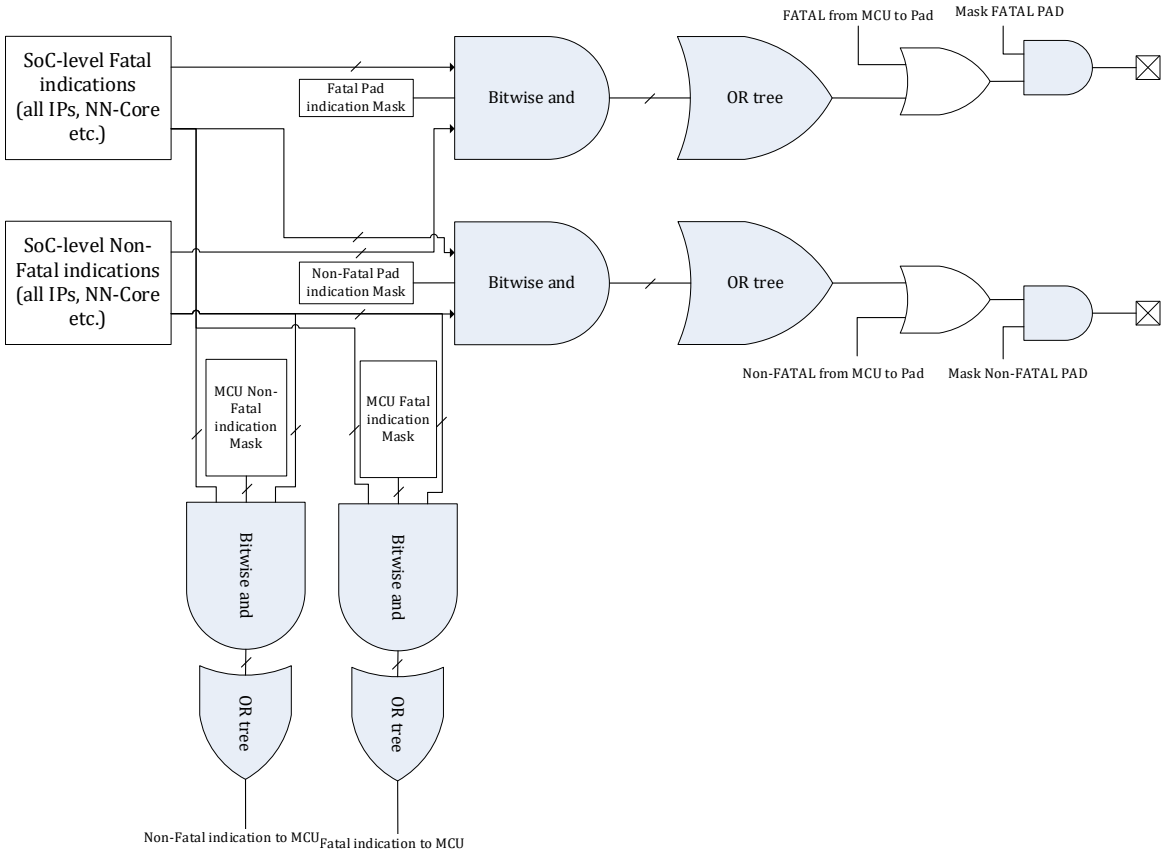


Figure 8 - SoC-Level Safety Aggregator

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